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Efficient Puncture and Non Puncture Architecture of Turbo Encoder on FPGA for Advanced Communication System

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Abstract -This paper concentrates on plan and execution in-vehicle framework chip with the help of efficient turbo encoder. This module is fostered with the help of FPGA implementation. Both sequential and equal calculations for the encoding strategy are contemplated. Basically two Methodologies were implemented. Fostering the equal calculation technique utilizing convey skip snake, it is shown that both chip size and handling time are gotten to the next level. The rationale usage is improved by diminished region. The Turbo encoder module is planned, recreated, and integrated utilizing Xilinx apparatuses. Xilinx vertex low power is utilized.

1. Introduction

It's undeniably true that remote correspondence frameworks are turning out to be more universal because of their compactness and portability with an assortment of improvements. In any case, as the quantity of clients proceeds to rise and the interest for better administrations requiring high transmission rates increments; a more pressing factor is put on the coding methods and regulation plans. As indicated by Shannon, expanding the transmission rate might limit mistake events as long as the rate was still beneath the channel limit. In an advanced transmission framework, blunder control is accomplished by the utilization of channel coding plans.[1-2] Channel coding plans help to decrease the BER and work on the dependability of data transmission. Turbo codes are a class of convolution codes whose exhibition as far as Bit Error Rate is near as far as possible by utilizing basic part codes and interleaves. Presently, 4G offers a high limit versatile media administration at 10^9 bit per second information , making it multiple times better compared to the third generation administrations. 5G New Radio (NR) is the looming improvement of flexible development expected to be utilized consistently in 2022 with a wide extent of comfort past the jobs of 4G[3-5].

2. Punctured Turbo Decoder

Puncturing [4] basically helps to increase data rate. The selection of upper encoder yields the odd part where as selecting the lower encoder yields the even part and it was recorded. In a more convoluted framework, penetrating tables are utilized.[6-7] A significant utilization of penetrating is to give inconsistent blunder insurance where moderately immaterial pieces or during cleaner channel conditions a lower rate coding is utilized by penetrating the coded bits while for more significant pieces or loud channel conditions, higher rate coding can be utilized.

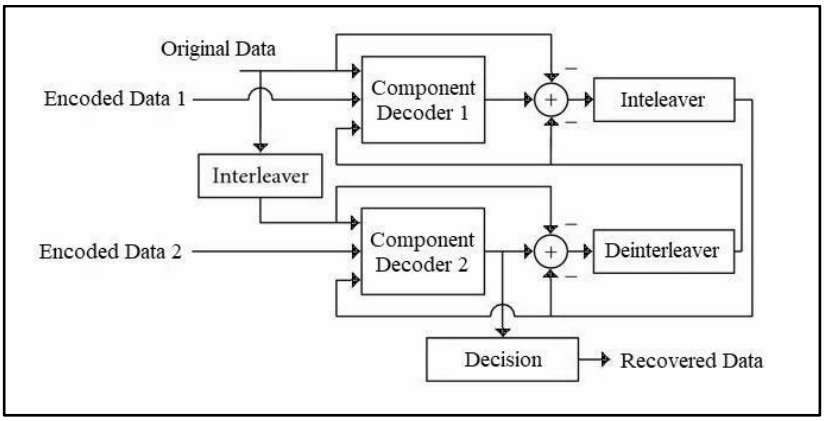

Figure 2. Block Diagram for Punctured Turbo Decoder (PTD)

The part decoders need to utilize these data sources and create delicate result. This implies that the decoder not just necessities to create the bitstream of the decoded arrangement yet in addition the likelihood of each decoded piece in the stream which is generally addressed by Log-Likelihood Ratio (LLR) whose extremity decides the piece sign and plentifulness communicates the likelihood. In our planned framework, one more approach to expanding rate and giving transmission capacity proficiency is taking advantage of a non-precise coding structure. [8-11]. As such, we simply think about equality (encoded) bits that secure 16-QAM tweak at first level then, at that point, penetrated then OFDM balanced. This model to accomplish rate 1/3, the planned design with penetrating that makes rate 1/4 is thought of. Then, at that point, methodical pieces are taken out; subsequently the rate increments to ⅓. This plan further develops execution for more modest square sizes contrasted with involving higher-request regulation for efficient bits.[12-15]

3. Non-Punctured Turbo Decoder

The non-penetrated super encoder as displayed in Figure 3., as introduced in [4], is an equivalent connection of two $(\frac{m}{m+1})$ rate RSC (Recursive Systematic Convolution) encoders disengaged by an interleaver which can be a S-erratic interleaved or a pseudorandom interleaver [9]. The mapper takes them purposeful pieces, one balance bit from the upper encoder, and the deinterleaved uniformity bit from the base encoder and maps them to 2m+2 glorious body centers. The plan of the Unpunctured gatherer is a decoder to choose the A Posteriori Probabilities (APP) of the conveyed pictures over an iterative unraveling process. The joined outward and exact information (Le&s) is taken out from the consequence of one

decoder and passed to the subsequent decoder as concluded information (La) to work on the unwavering quality of the subsequent decoder's result as well as the other way around.

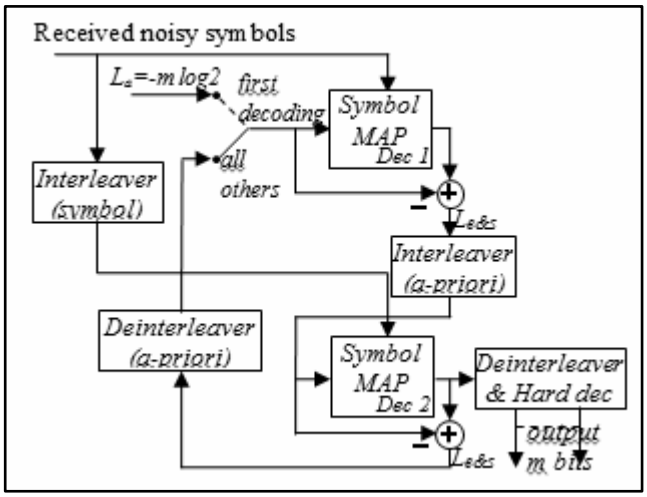

Figure 3. Structure of the Unpunctured Turbo Decoder (UNPTD)

4. Turbo Encoder Module

This module gives a strategy to the advance communication process through FEC technique. The IVS uses a Turbo encoder module with 1=3 code rate. The Turbo encoder functionalities are quick and dirty in the third time affiliation project (3GPP) rules. The 3GPP Turbo encoder is illustrated in Figure 4.1. The data indication of the super encodes is the MSD data appended with the CRC correspondence bits in equal. The square length of the MSD data is 1148 pieces. The consequence of the module is the MSD encoded data in matched. Executing the super coding system with 1=3 coding rate and invigorates bits, the length of the outcome is 3456 pieces. The surges structure has an impact of the Turbo encoder.[16-18]

The Turbo encoder utilizes an equal linked convolution code (PCCC). The PCCC includes two constituent encoders with eight states as it is shown in Figure 4.1. The fundamental status of the register are zeros. The features of MSD Pieces utilized while using convolutional method. The parity bit 1 is require for the consistent indistinguishable strategy of the main constituent. The requirement of MSD bits after the interleaved while using 3GPP intereaved method.[19-20]

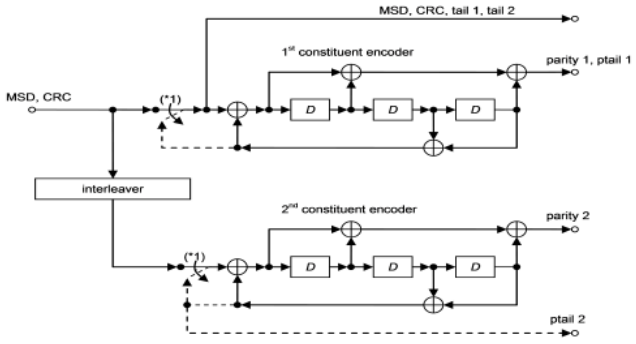

Fig. 4.1: The structure of the Turbo encoder.

The number of pieces of information for parity bit 1 and 2 is of 1148. The trailing bit which is added to the information of 12 identical pieces. The input of the shift register is provided with the trailing bits for further processing.[20-22] The arrangement of the output of the encoder is shown in Figure4.2.

Fig. 4.2: Output of Encoder.

4.1 Interleaver

The relationship of the PCCC has been discussed as follows:

$$G(D) = \left(1, \frac{g_1(D)}{g_0(D)}\right) \quad (1)$$

where

$$g_1(D) = 1 + D^2 + D^3$$

$$g_0(D) = 1 + D + D^3$$

Let us consider a set of input bits to encoder $x_1, x_2, ..., x_K$, where as interleaver output is $x'_1, x'_2, ..., x'_K$, and the set of constituents as $z_1, z_2, ..., z_K$ and $z'_1, z'_2, ..., z'_K$, respectively; Number of inputs to turbo encode is K.

Resultant of the process is given with a representation

$$d_K^{(0)} = x_K, d_K^{(1)} = z_K, d_K^{(2)} = z'_K$$

where $K = 0, 1, ..., K - 1.$

Let us consider blocks of three coded output is, $d_K^{(0)}$, $d_K^{(1)}$, and $d_K^{(2)}$, K indicate the lattice number. The grid pieces are delivered the large number of data bits.. The output of encoding process which can inferred as :

$$d_K^{(0)} = x_K, \quad d_{K+1}^{(0)} = z_{K+1}, \quad d_{K+2}^{(0)} = x'_K, \quad d_{K+3}^{(0)} = z'_{K+1}$$

$$d_K^{(1)} = z_K, \quad d_{K+1}^{(1)} = x_{K+2}, \quad d_{K+2}^{(1)} = z'_K, \quad d_{K+3}^{(1)} = x'_{K+2}$$

$$d_K^{(2)} = x_{K+1}, d_{K+1}^{(2)} = z_{K+2}, d_{K+2}^{(2)} = x'_{K+1}, d_{K+3}^{(2)} = z'_{K+2}$$

where $K = 0, 1, ..., K - 1.$

For the purpose of execution the value of K has been set a range of 40<K<5114. In any case, the data bits are re-coordinated in a system structure with the help of turbo coder that has segment, C, and line, R. Number of lines represented as 0,1,… ,R - 1 and the fragments are facilitated as 0,1,… ,C-1. The amounts of lines despite everything up in the air as shown by the 3GPP standard for Turbo encoder interleavers. Then the input bits $x_1, x_2, ..., x_K$ are re-organized in a matrix where $y_k = x_k$ for k = 1,2,…,K and $y_k = 0$ for the elements that $R \times C > K$:

$$\begin{bmatrix} y_1 & y_2 & y_3 & \cdots & y_C \\ y_{(C+1)} & y_{(C+2)} & y_{(C+3)} & \cdots & y_{(C+C)} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ y_{((R-1)C+1)} & y_{((R-1)C+2)} & y_{((R-1)C+3)} & \cdots & y_{(R\times C)} \end{bmatrix}$$

Then, at that point, an intra-column and between line change is performedon the R X C network. The equation justify the relationship of permutation pattern

$$s(j) = (v \times s(j-1)) \mod p \qquad (2)$$

Where $\langle s(j) \rangle$ for $j \in 1, 2, ..., p-2$ and p(0) = 0 is the intarow permutation sequence and v is associated primitive root for the specified p from table 4.1 . The table 4.1 discuss about the various permutation of intra-row. The index has been assigned with various element of RXC. Also the minimum prime integer (qi) is determined in the sequence q(i) for $i \in 0, 1, ..., R-1$ such that qi > q(i-1), qi > 6 and g.c.d(qi, p - 1) = 1, where g.c.d is the greater common divisor. Then one can build a sequence of the permuted prime integers D r(i) for $i \in 0, 1, ..., R-1$ such that,

Table 4.1: 3GPP inter-row permutation pattern

K	*R*	Inter-row permutation patterns <*T*(0), *T*(1), …, *T*(*R* - 1)>
(40 ≤ *K* ≤ 159)	5	<4, 3, 2, 1, 0>
(160 ≤ *K* ≤ 200) or (481 ≤ *K* ≤ 530)	10	<9, 8, 7, 6, 5, 4, 3, 2, 1, 0>
(2281 ≤ *K* ≤ 2480) or (3161 ≤ *K* ≤ 3210)	20	<19, 9, 14, 4, 0, 2, 5, 7, 12, 18, 16, 13, 17, 15, 3, 1, 6, 11, 8, 10>
K = any other value	20	<19, 9, 14, 4, 0, 2, 5, 7, 12, 18, 10, 8, 13, 17, 3, 1, 16, 6, 15, 11>

For the intra row representation the relation has been discussed below as,

$$U_i(j) = s((j \times r_i) \mod (p-1)) \quad (3)$$

where $j = 0, 1, ..., (p-1)$ and $U_i(p-1) = 0$.
if $(C = p+1)$ then,

$$U_i(j) = s((j \times r_i) \mod (p-1)) \quad (4)$$

where $j = 0, 1, ..., (p-1)$, $U_i(p-1) = 0$, and $U_i(p) = p$.
if $(C = p-1)$ then,

$$U_i(j) = s((j \times r_i) \mod (p-1)) - 1 \quad (5)$$

where $j = 0, 1, ..., (p-1)$.

The resultant output of R X C matrix is denoted by $y'_k = y_k$ such that:

$$\begin{bmatrix} y'_1 & y'_{(R+1)} & y'_{(2R+1)} & \cdots & y'_{((C-1)R+1)} \\ y'_2 & y'_{(R+1)} & y'_{(2R+2)} & \cdots & y'_{((C-1)R+2)} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ y'_R & y'_{(2R)} & y'_{(3R)} & \cdots & y'_{(R\times C)} \end{bmatrix}$$

The interleaver output can be determined with the relation, $x'_2, x'_2, ..., x'_K$ K, y'_1 and $y'_{(R\times C)}$. indicate the specific element of the matrix.

The size of matrix for the matrix is selected as 20x58. The going with progresses are done to drive the interleaver network:

1. Number of bits are indicated as b1, b2,… , bK, where bK = BK and K = 1148. The excess components are cushioned with zeros.

2. The intra-column and between line stage are performed by 3GPP.

3. The determined components of the interleaver lattice, with the exception of the cushioned pieces, are put away in a record in hexadecimal configuration.

The turbo encoder is incorporated in VHDL . The above process has been analysed in hexadecimal file with all the consideration made for the effective process. According to the 3GPP standards , the interleaver matrix is a RXC rectangular matrix, where R is the number of rows and C is the number of columns. The size of the matrix is 20 X 58. The following steps are implemented to drive the interleaver matrix:

Step 1: The info bits of the grid are indicated as b1, b2,… , bK,where bK = BK and K = 1148.

Step 2. The intra-column and between line stage is performed by 3GPP .

Step 3. The determined components of the interleaver lattice, with the exception of the cushioned pieces, are put away in a record in hexadecimal organization.

4.2 The serial computation method

In the wake of playing out the encoding, it creates the result bits. Albeit the strategy is planned and carried out, it is noticed that there is a long handling time that can be covered with different cycles in the module..

Ts indicate the pre- processing time period for the serial computation,

$$T_s = T_r + T_b + T_{parity1} + T_{tail1} + T_{parity2} + T_{tail2} + T_w \qquad (1)$$

$$T_s = 1148 + 1148 + 1148 + 3 + 1148 + 3 + 3456 = 8054$$

where Tr - reading time period of 1148 bits, Tb- bit period required to build the register after execution, T_{parit1} - processing time period of parity bit , T_{tail} tail bit execution period, and T_w is execution time period.

4.3 The parallel computation method

Various cycles encountered when sequential calculation procedure covered while utilizing equal registering method. There are two capacities created in the equal Turbo encoder. The two capacities carries out practically all the handling season of the encoding procedure. There are various time period has been focused to discuss the sequential time period represented as

$$T_s = T_r + T_b + T_{parity1} + T_{tail1} + T_{parity2} + T_{tail2} + T_w$$

$$T_s = 1148 + 1148 + 1148 + 3 + 1148 + 3 + 3456 = 8054$$

For a complete cycle of execution of parallel computation method the relations has been discussed as follows

$$T_p = 1 + T_w = 1 + 3456 = 3457 \qquad (2)$$

Then one has,

$$T_p = 0.42T_s \qquad (3)$$

5. Proposed Design

The proposed design has been incorporated with FPGA . This advancement in the schematic representation of RTL circuit which enhance the time period of execution.. The HDL language associated with the coding technique with respect to the blocks of bits and helps in better investigating. The figure5.1 discuss the complete schematic of planning for execution.

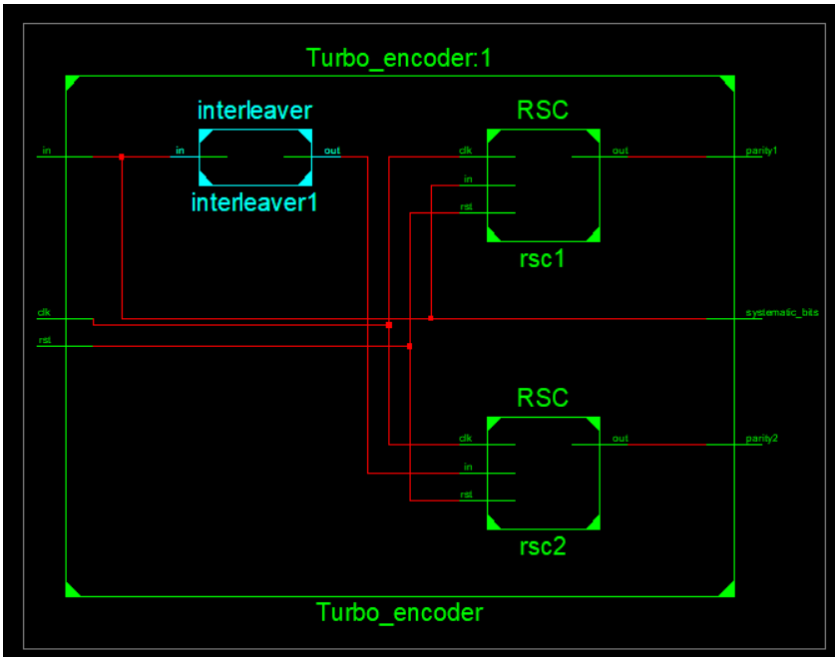

Figure 5.1: RTL schematic of turbo encoder

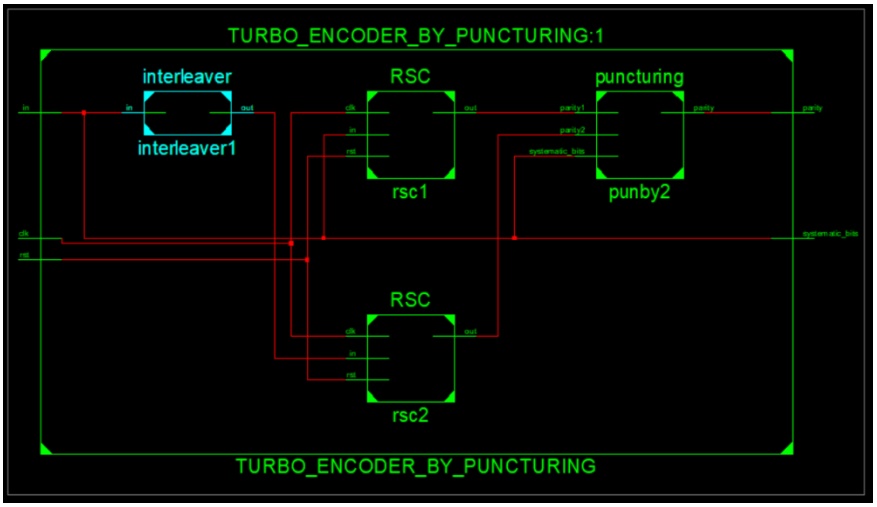

Figure 5.2 : RTL schematic of turbo encoder by puncturing

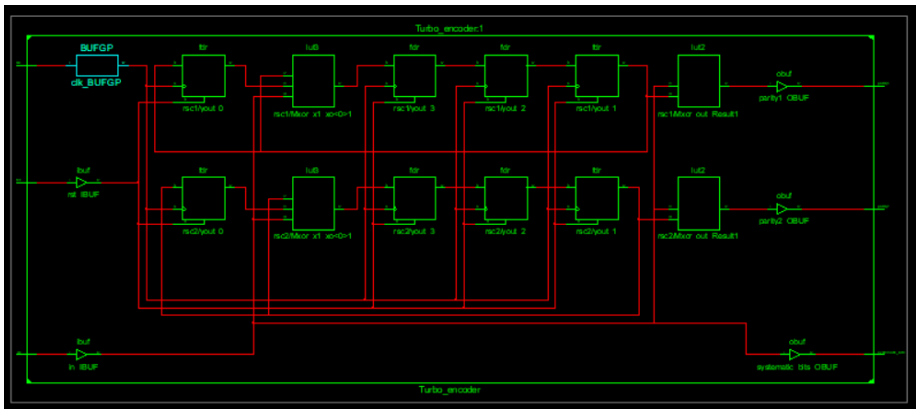

Figure 5. 3: view technology schematic view of Turbo encoder

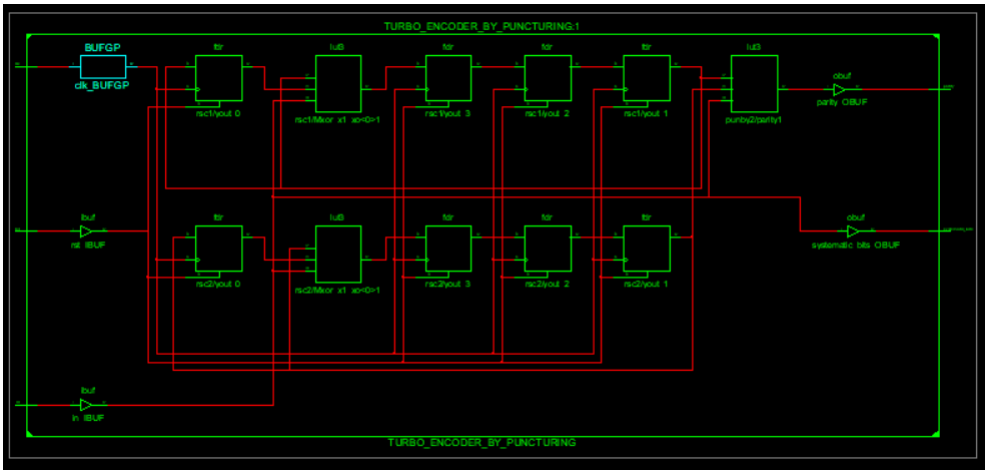

Figure 5.4: view technology schematic view of Turbo encoder by puncturing

Parameters of Non Puncturing Turbo Encoder:-

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	4	960	0%
Number of Slice Flip Flops	8	1920	0%
Number of 4 input LUTs	4	1920	0%
Number of bonded IOBs	6	66	9%
Number of GCLKs	1	24	4%

Minimum period: 1.875ns (Maximum Frequency: 533.234MHz)

Minimum input arrival time before clock: 2.676ns

Maximum output required time after clock: 5.255ns

Maximum combinational path delay: 5.851ns

Parameters of Puncturing Turbo Encoder:-

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	4	960	0%
Number of Slice Flip Flops	8	1920	0%
Number of 4 input LUTs	3	1920	0%
Number of bonded IOBs	5	66	7%
Number of GCLKs	1	24	4%

Minimum period: 1.875ns (Maximum Frequency: 533.234MHz)

Minimum input arrival time before clock: 2.637ns

Maximum output required time after clock: 5.172ns

Maximum combinational path delay: 5.895ns

Measured parameters	Turbo encoder	Turbo decoder
Number of Logic gates	51	35150
Number of registers	41	24243
Total pins	8	8
Core static thermal power dissipation	51.81 mW	79.93 mW
`Input/output thermal power dissipation	34.06 mW	30.93 mW
Total power	85.87 mW	110. mW
Maximum frequency	313.97M H	75.06 MH

6. Comparison with Existing Design

The table discuss about the comparative study with the existing design. It also discuss about the various verticals to justify the design is improvise version and helps in advance communication system.

Table 6.1 Comparison With Existing Model

Parameters	**Existed turbo decoder**	**Proposed turbo decoder**
No of registers	24243	10355
Frequency (MHz)	75.06	554.921

Table 6.2 Comparison with respect to methodology

Methodology used in encoding	**Puncturing,non-puncturing,serial and parallel computations**
Decoding algorithm	SOVA
Bit length	1148

Inter leaver type	random interleaver
Channel	AWGN (Additive White Gaussian Channel

7. Conclusion

The Turbo encoder module is arranged and executed to be an embedded module in the IVS modem. FPGA progresses are used to cultivate the Turbo encoder module. Xilinx gadgets and Verilog HDL are used to design and reenact the module. with entering and non-infiltrating methods are perused up for the encoding framework. It is demonstrated the way that the entering can additionally foster the chip size of the module. Contrasting and the penetrating and non-penetrating strategies, the penetrating encoding, utilizing less number of LUTs.

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