Study of Performance of Low Power High-Speed Hybrid in 1-Bit Full Adder Circuit

Dr. Vijay Prakash Singh,

Research Guide, Dept. of Electronics and Communication Engineering, Sri Satya Sai University of Technology & Medical Sciences, Sehore, Bhopal-Indore Road, Madhya Pradesh, India

Latha Yallanki

Research Scholar, Dept. of Electronics and Communication Engineering, Sri Satya Sai University of Technology & Medical Sciences, Sehore, Bhopal-Indore Road, Madhya Pradesh, India

Article Info
Page Number: 519-528
Publication Issue:
Vol. 71 No. 2 (2022)

Article History
Article Received:
25 December 2021
Revised: 20 January 2022
Accepted: 24 February 2022
Publication: 28 March 2022

Abstract
In this review, a proposed 1-cycle cross breed full snake design is made sense of utilizing both the corresponding CMOS hypothesis and the transmission entryway hypothesis. The plan is executed for a 1-cycle swell convey snake prior to being extended for a 64-bit swell convey viper. The circuit is executed utilizing Coach Graphics' 130nm innovation . Presentation boundaries such as region, complete power distribution, and power postpone item (PDP) were compared to existing plans such as conventional CMOS full adders (CMOS), complementary pass semiconductor adders (CPL), HPSC full adders, low energy HPSC full adders, transmission capability full adders (TFA), and changed 1-bit hybrid full adders. Due to the deliberate aggregation of incredibly weak CMOS inverters mixed with areas of strength for with entryways, the usual power utilisation for 1V stockpile at 130-nm innovation is considered as exceptionally low with modestly low postponement. The design has been extended for both 32-bit and 64-bit full adders, and it is believed to operate effectively with reduced delay and less power dispersion at 130-nm technology for 1V Supply voltage. In contrast with prior full viper plans, the mixture snake offers critical headways concerning power, district, and speed.

Keywords— power high-speed, speed hybrid, 1-bit, adder circuit, speed, power,

1. Introduction

In intricate computing and number-crunching circuits like multipliers, comparators, and equality checkers, adders play a crucial role. Various methodologies have as of late been advanced to carry out a low power full snake. (C.-K. Tung, 2007,)The most frequently utilized and generally involved circuits in extremely enormous scope coordination (VLSI) models are speedy number related calculation cells, including adders and multipliers.

Specifically, calculating circuits (adders and multipliers), comparators, fairness checkers, code converters, blunder perceiving, then again, mistake amending codes, and stage finders all utilization XOR-XNOR circuits as key structure blocks. The crucial structure block of mind boggling numerical circuits like development, rise, division, exponentiation, and so on is the viper. Inquiries for the circuit incorporate the quantity of reversal levels, the quantity of

semiconductors associated in series, the estimations of the semiconductors (i.e., the channel widths), and the intra-cell wire capacitances. (H. Chang, 2005)The size of the circuit is impacted by the amount, creation, and intricacy of the wire. Some use a single rationale plan for the execution of the whole adder, whilst others use many rationale plans. One of the most important resources is power, so when designing a framework, fashioners try to reduce power. The exchanging motion, hub capacitances (composed of entryway, dissemination, and wire capacitances), and control circuit size all affect power scattering. By selecting the proper W/L ratio, it is possible to restrict power distribution without lowering stockpile voltage. Different rationales have a propensity to favour one execution perspective over another. One-bit and modified one-bit hybrid full adders are envisaged for this paper. The Carry age module and XNOR are both included in the proposed hybrid full adder.

VLSI and super enormous scope availability methods are expected by the ascent in the utilization of battery-worked versatile gadgets such cell phones, individual computerized colleagues (PDAs), and diaries. Full adders, one of the main parts of all the previously mentioned circuit applications, have kept on being an intriguing issue of exploration . (K. Yano, 1996.) For the implementation of 1-bit complete adder cells, various types of logic, each with advantages and disadvantages, were considered. The already-publicized proposals can be generally divided into two categories: A static style; a distinctive style Static full adders, on the other hand, are frequently more dependable, user-friendly, and economical with energy. The on chip space need is frequently higher than its dynamic relative.

2. Review of Full Adder Topologies

To operate 1-bit adder cells, a few versions of distinct rationale approaches have recently been developed. M. M. Vai 2001 In the case of a logical structure, there are two different types of complete adders. The other is a dynamic style, while the first is static. In general, static full adders are more dependable, easier to use, and use less power than dynamic ones. Another rationale style to consider when planning a rationale capability is dynamic. It enjoys a couple of upper hands over the static mode, for example, higher trade rates, no static power use, nonratioed thinking, going full bore voltage levels, and less semiconductors. In contrast to the normal CMOS rationale, which calls for 2N semiconductors, a N input rationale capability requires N+2 semiconductors. The area advantage results from the fact that a particular CMOS entryway's pMOS organisation only consists of one semiconductor. The postpone advantage is based on a reduction in the capacitive burden at the result hub, which is also a result of this. (M. Aguirre-Hernandez, 2011.)The whole adder has a variety of problems, including power usage, execution, region, commotion resistance, consistency, and fantastic driving ability. Various inspectors have consolidated these two thoughts, and they have since prompted blending dynamic-static full adders. They looked into many research approaches and realised that each viper using CMOS technology has advantages and disadvantages.

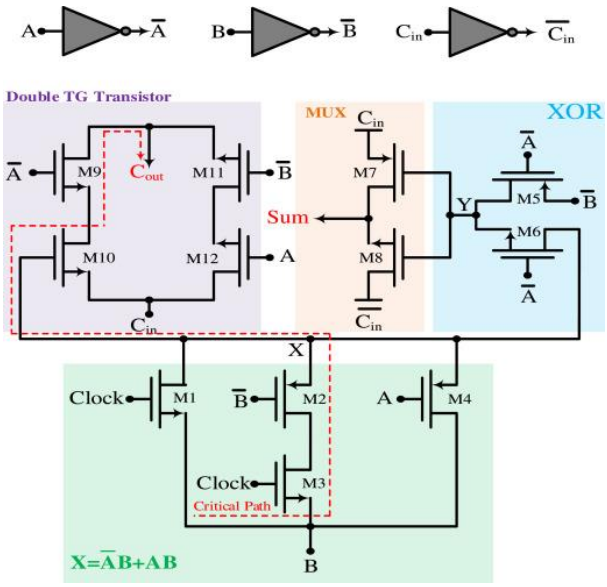

Figure: 1 TG-Pseudo adder cell.

The pseudo nMOS full adder cell operates on ratioed style, also known as pseudo reasoning. 14 semiconductors are used in this entire adder cell to demonstrate the negative expansion capabilities. Pseudo-nMOS adder cells have the advantage of being faster (than regular complete adders) and having fewer semiconductors. The reduced yield voltage swing and increased static power consumption of the semiconductor in a pseudo-nMOS cell make this adder cell more susceptible to disturbance. This circuit has a CMOS inverter to increase the outcome swing.

As shown in Figure 1, the recently developed complete adder S. Wairya 2010 is a combination of pseudo nMOS entryways and low power transmission doors. A particular sort of pass-semiconductor rationale circuit, known as a transmission entryway, comprises of a pMOS semiconductor and a nMOS semiconductor that are associated in equivalent measure. Although there is no voltage loss at the yield hub, twice as many semiconductors are needed to achieve the same amount of capacity.

The Complementary Pass Transistor Rationale (CPL) with swing reclamation, which makes use of 32 semiconductors, is another full adder. H. Hara, 1994 Additionally, their supplement develops numerous intermediary hubs for CPL Adder to provide the desired results. The fundamental components of CPL include the low yield voltage swing at the inner hub and the small stack level, both of which reduce power consumption. Due to the consequence inverters' doors' low swing, the CPL experiences static power utilisation. CPL is related to the swing re-established pass-semiconductor reasoning (SRPL) developed by A. Parameswar in 1996 and the double pass-semiconductor rationale (DPL) [8].

2 Design Methodologies for the Suggested Full Adder

The entire adder circuit being proposed is addressed using threeblocks, as shown in Fig. 1. (a). Modules 1 and 2 of the XNOR architecture create the aggregate sign (SUM), while Module 3 creates the result convey signal (Cout). Each module is uniquely created to

guarantee that the power, deferral, and region of the complete adder circuit are optimised. These courses are thoroughly detailed below.

A. Modifie XNOR Module

The XNOR module is primarily responsible for the proposed complete adder circuit's high power consumption. As a result, the objective of this module is to maintain the voltage while consuming the least amount of power possible. Figure 1(b) depicts the newly constructed XNOR circuit, where the deliberate use of a weak inverter considerably reduces power consumption (small channelwidth of semiconductors).

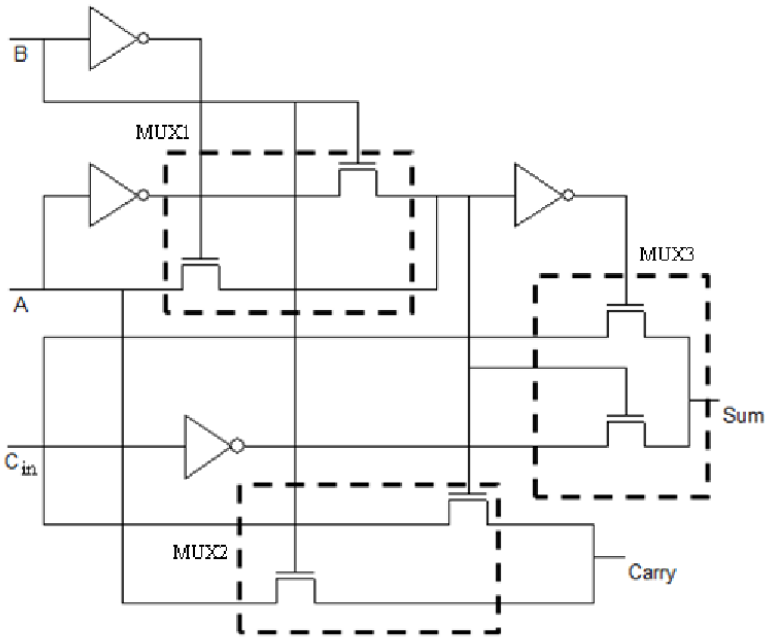

Figure: 1 Diagram showing the proposed complete adder in more detail.

Mn1 is also shown [Fig. 1(b)]. Semiconductors Mn3 and MP3 for level re-establishing [Fig. 1(b)] ensure that the output signal swings in all directions. The XOR/XNOR geographies in and have previously been discussed. Four semiconductors are used in the XOR and XNOR devices described in, albeit at the cost of a minor logic swing. Six transistors are actually used in the XOR/XNOR mentioned in order to outperform four TXOR/XNOR in terms of logic swing. Although the 6 T XOR/XNOR module used in this study also used 6 T, it did so using a different semiconductor manufacturing process. The muddy XNOR reported in this research provides low-power and rapid performance in comparison to 6 T XOR/XNOR (with acceptable logic swing).

B. Module for Convey Generation

The suggested circuit, as shown in Fig. 1, employs the semiconductors Mp7, Mp8, Mn7, and Mn8 to execute the result convey signal. (c). The entire information transfer spread is considerably reduced since the information transfer signal (Cin) only propagates through one transmission door (Mn7 and Mp7). the deliberate use of strong transmission doors, which are

dependable and limit the spread deferral of the convey signal farther (Mn7, Mn8, Mn8, and Mp8 transistors produce enormous channel width)

3. Full Adder Operation with the Proposed Simulation Test Bench Setup

The planned full adder's detailed outline can be seen in Fig. 2. The whole adder's aggregate result is executed by XNORmodules. The controlled inverter using the semiconductor pair Mp1 and Mn2 is planned using the B' that the inverter using Mp1 and Mn1 generates. The XNOR of An and B is the controlled inverter's main output. (M. Shams and M. A. Bayoumi, , 2000.)In any case, two pass semiconductors, Mn3 and MP3, were used to overcome a voltage corruption problem. nMOS semiconductors and MP4, MP5, and MP6 PMOS transistors (Mn4, Mn5, and Mn6) must be able to comprehend the later stage XNOR module in order to fully realise the SUM capabilities. The following Cout age condition was identified when a complete adder's reality table was dissected:

$$\boldsymbol{IF, A = B, Then\ C_{out} = B; else, C_{out} = C_{in}}$$

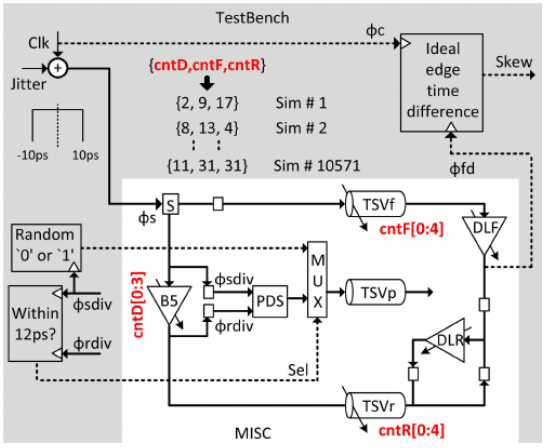

Figure: 2 Setup for a simulation test bench

A capability confirms the equality of inputs An and B. If they are identical, Cout uses the transmission entryway identified by transistors Mp8 and Mn8 to carry out the same task as B. The information convey signal (Cin) is yet rejected as Cout by a different transmission gateway composed of the semiconductors Mp7 and Mn7. The inability of a single bit adder cell created for maximum performance to function effectively in organisational contexts makes sense. This is because it's possible that when coupled in a cascaded fashion, the driver adder cells won't provide the determined cells the right input signal level. The cumulative signal level degradation at low inventory voltages may lead to inaccurate results and circuit failure. In order to disassemble the proposed complete adder while it is really being utilised in VLSI applications, a useful replica environment is constructed, as illustrated in Fig. 3. Cushions are put at the information and results of the exam seat to provide a comfortable environment. . To achieve optimal stacking conditions, the results are additionally stacked with cradles. The supports manage adder cell contributions and account for the impact of information capacitance. Several test bench setups are used to reconstruct the indicated complete adder. The usual prototype for these test seats includes two cradles and three cushions (Fig. 3). They just changed the amount of adder cell phases between the simulation

setup's input and output. There were different levels that got bigger and bigger starting with two. After the third step, the convey propagation time from the contribution to the result in the request for two began to climb considerably (made sense of in detailing Section IV-B). For usage in reenactments, the three-stage reproduction test bench is adopted. The behaviour of the execution constraints (power and deferral) for the second adder cell may also be assessed using this test bench. By employing the output and feedback capacitances of surrounding adder cells as their input capacitances, the tested adder cell was able to continuously use the cascaded technique. The data sources were given different arbitrary sign instances, and the most pessimistic case was used to reflect the research and comparison findings for the second full adder cell. For both the 180 nm and 90 nm improvements, the exhibition evaluation of the proposed full adder was conducted using a fluctuation in supply voltage.

4. Analysis of the suggested complete adder's performance

With a focus on the hybrid plan approach, the suggested full was recreated employing both 90- and 180-nm innovation and contrasted with the other probable adder plans mentioned in.

Transistor Name	190mm Technology		100mm Technology	
	Size (w) (nm)	Distance (L) (nm)	Size (w) (nm)	Distance (L) (nm)
Mn2, Mn7	500	190	150	100
Mn2, Mn7	900	190	340	100
Mn3, Mn4	500	190	150	100
Mn3, Mn4	900	190	460	100
Mp5, M6	500	190	150	100
Mp5, M6	500	190	150	100
Mn8, Mn9	500	190	460	100
Mn8, Mn9	500	190	700	100

Table: 1 Transistor Sizes of Proposed Full Adder

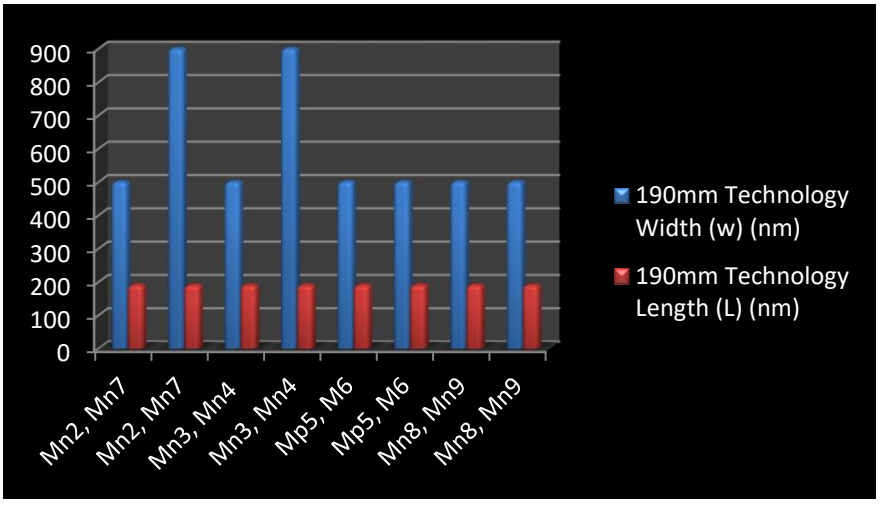

Figure: 3 Transistor Sizes of 190 mm Technology

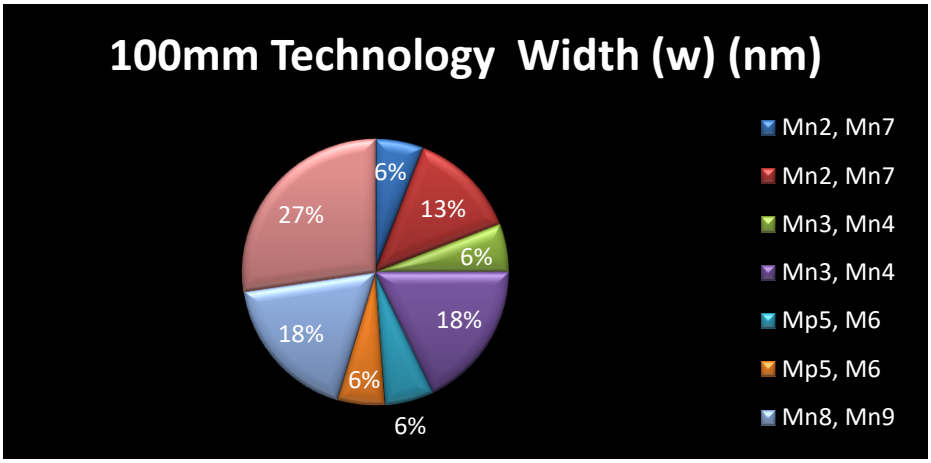

Figure: 4 Transistor Sizes of 100 mm Technology

Design	Average Strength (um)	Delay (um)	PDP (D)	Transistor Number
C-CMOS	7.220	393.02	1.917842	30
Mirror	7.0798	992.72	2.714105	30
CPL	8.81986	193.98	2.52023	35
TFA	9.2592	393.62	3.398517	18
15 T	9.4820	142.603	3.9090	25
11 T	13.8218	274.8	5.96688	15
HPSC	15.3550	189.5	2.903063	12
Majority Based	7.3899	374.3	2.75716	25
25 T	7.3298	187.5	2.27333	-
FA- Hybrid	16.92	414.3	5.990	25

Table: 2 Results of Full Adders Simulation in 1.8 V Supple with 180 Nm Technology

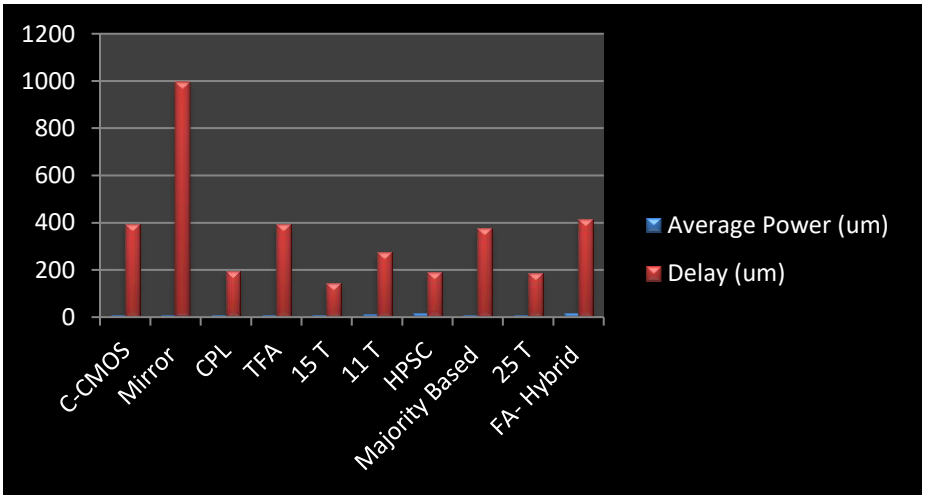

Figure: 5 Results of Full Adders Simulation in 1.8 V Supple with 180 Nm Technology

In the recommended scenario, the power-postpone item (PDP), or the quantity of energy utilised, has been limited with the hope of advancing both power and deferring the circuit. The power consumption of the current plan could be reduced by basically evaluating the semiconductors in inverter circuits, and the convey spread postponement could be improved by estimating the semiconductors of the transmission entryways situated between the methods from Cin to Cout. For both technologies, Table I lists the semiconductor sizes for the proposed entire adder circuit (90 and 180 nm). Tables II I for 180-nm and 90-nm innovation individually offer information on the proposed full adder's power consumption, propagation delay, and PDP as well as comparisons with currently available full adders (from authoring).

5. Execution of a 32-Bit Full Adder

A 32-bit convey engendering adder is added to the suggested 1-bit complete adder (Fig. 8(a)). In this non-carry look-ahead adder structure, the convey engendering lasts up until the last adder block. Additionally, both with and without the use of intermediate buffers at the necessary stages, the performance of this 32-bit adder was assessed in 180- and 90-nm technologies. The appropriate adder stages' final output was used to complete the fuse (5). the exercise of authority and the growth of communication

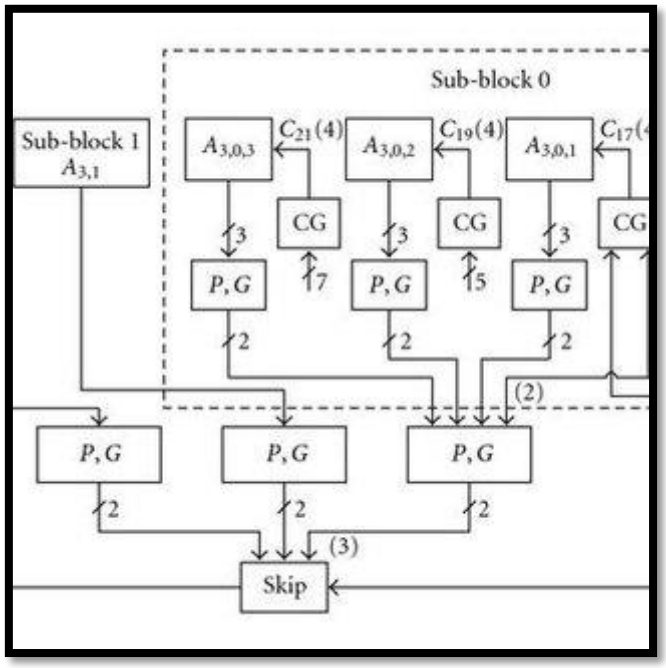

Figure: 6 A 32-bit full adder is possible using a 1-bit full adder. (b) A 32-bit carry propagation adder's power and delay performance with and without a buffer when powered by voltages of 1.8 V and 1.2 V for 180 nm and 90 nm, respectively. At

The delay continued to develop when the cradle was used, but the improvement in the delay was more noticeable. With supply voltages of 1.8 V (90-nm technology) and 1.2 V (180-nm innovation), Figure 8 illustrates the performance of this 32-bit full adder at 100 MHz (b). In 180-nm innovation, the distinction between static and dynamic power consumption is significant. In any case, the rise of the sub threshold conduction current and door leaking

caused this differential in 90-nm technology to be significantly reduced. The carry generating delay's behaviour when extended from 1 to 32 bits is shown in Figure 8(c). It was noted that the convey proliferation latency increased almost exponentially as a result of the proposed 1-bit full adder.

6. Conclusion

This project proposes a low-power 1-bit hybrid full adder, and the concept has been enhanced to incorporate a 64-bit ripple convey adder (RCA). CMOS, CPL, TFA, HPSC, and LEHPSC designs are just a few examples of popular design techniques that are contrasted with each other in the simulations, which are carried out using Mentor design tools with 130-nm technology. (M. Shams and M. A. Bayoumi, "Structured approach for designing low power adders," in Proceedings of the 31st Asilomar Conference on Signals, Systems & Computers, vol. 1, pp. 757–761, November , 1997.)The reproduction results show that the proposed adder gives a more sophisticated PDP in contrast to the preceding reports. The effective coupling areas of strength for doors driven by weak CMOS inverters result in quick swapping speeds. CMOS, CPL, TFA, TGA, and other hybrid designs were compared to the simulation's use of well-known Cadence Virtuoso tools using 180/90-nm technology. The reproduction results demonstrated that the PDP offered by the proposed adder was superior as compared to the preceding reports. With the efficient coupling of strong areas of strength for of entryways powered by weak CMOS inverters, quick exchanging speeds (224 ps at 1.8-V inventory) are reached for a layout area of 102.94 m2 (in 19-nm innovation) excluding buffer.

References

1. C.-K. Tung, Y.-C. Hung, S.-H. Shieh, G.-S. Huang,"A lowpower high-speed hybrid CMOS full adder for embedded system", In Proc. IEEE Conf. Design Diagnostics Electron. Circuits Syst., Vol. 13. Apr. 2007, pp. 1–4.
2. H. Chang, J. M. Gu, M. Zhang,"A review of 0.18-μm full adder performances for tree structured arithmetic circuits", IEEE Trans. Very Large Scale Integr. (VLSI) Syst., Vol. 13, No. 6, pp. 686–695, Jun. 2005.
3. K. Yano, Y. Sasaki, K. Rikino, and K. Seki, "Top-down passtransistor logic design," IEEE Journal of Solid-State Circuits, vol. 31, no. 6, pp. 792–803, 1996.
4. M. Aguirre-Hernandez, M. Linares-Aranda,"CMOS fulladders for energy-efficient arithmetic applications", IEEE Trans. Very Large Scale Integr. (VLSI) Syst., Vol. 19, No. 4, pp. 718–721, Apr. 2011.
5. M. L. Aranda, R. Báez, O. G. Diaz,"Hybrid adders for highspeed arithmetic circuits: A comparison", In Proc. 7th IEEE Int. Conf. Elect. Eng. Comput. Sci. Autom. Control (CCE), Tuxtla Gutierrez, NM, USA, Sep. 2010, pp. 546–549.
6. M. Shams and M. A. Bayoumi, "A novel high-performance CMOS 1-bit full-adder cell," IEEE Transactions on Circuits and Systems II, vol. 47, no. 5, pp. 478–481, 2000.
7. M. Shams and M. A. Bayoumi, "Structured approach for designing low power adders," in Proceedings of the 31st Asilomar Conference on Signals, Systems & Computers, vol. 1, pp. 757–761, November 1997.

8. M. Vesterbacka,"A 14-transistor CMOS full adder with full voltage-swing nodes", In Proc. IEEE Workshop Signal Process. Syst. (SiPS), Taipei, Taiwan, Oct. 1999, pp. 713–722.

9. M. Zhang, J. Gu, C.-H. Chang,"A novel hybrid pass logic with static CMOS output drive full-adder cell", In Proc. Int. Symp. Circuits Syst., May 2003, pp. 317–320.

10. Parameswar, H. Hara, and T. Sakurai, "A swing restored pass-transistor logic-based multiply and accumulate circuit for multimedia applications," IEEE Journal of Solid-State Circuits, vol. 31, no. 6, pp. 804–809, 1996.

11. Partha Bhattacharyya, Bijoy Kundu, Sovan Ghosh, Vinay Kumar, Anup Dandapat,"Performance Analysis Of a LowPower High-Speed Hybrid 1-bit Full Adder circuit", 2014.

12. R. Zimmermann and W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," IEEE Journal of Solid-State Circuits, vol. 32, no. 7, pp. 1079–1090, 1997.

13. Radhakrishnan, "Low-voltage low-power CMOS Full Adder," IEE Proceedings: Circuits, Devices and Systems, vol. 148, no. 1, pp. 19–24, 2001.

14. Radhakrishnan, S. R. Whitaker, and G. K. Maki, "Formal design procedures for pass-transistor switching circuits," IEEE Journal of Solid-State Circuits, vol. 20, no. 2, pp. 531–536, 1984.

15. Radhakrishnan,"Low-voltage low-power CMOS full adder", IEEE Proc.-Circuits Devices Syst., Vol. 148, No. 1, pp. 19–24, Feb. 2001.

16. S. Goel, A. Kumar, and M. A. Bayoumi, "Design of robust, energy-efficient full adders for deep-submicrometer design using hybrid-CMOS logic style," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 14, no. 12, pp. 1309–1321, 2006.

17. S. Goel, A. Kumar, M. A. Bayoumi,"Design of robust, energy-efficient full adders for deep-submicrometer design using hybrid-CMOS logic style", IEEE Trans. Very Large Scale Integr. (VLSI) Syst., Vol. 14, No. 12, pp. 1309–1321, Dec. 2006.

18. S. Goel, M. Elgamel, M. A. Bayoumi,"Novel design methodology for high-performance XOR-XNOR circuit design", in Proc. 16th Symp. Integr. Circuits Syst. Design (SBCCI), Sep. 2003, pp. 71–76 C.-K. Tung, Y.-C. Hung, S.-H. Shieh, and G.-S. Huang, "A low-powerhigh-speed hybrid CMOS full adder for embedded system,"

19. S. Goel, S. Gollamudi, A. Kumar, and M. Bayoumi, "On the design of low-energy hybrid CMOS 1 -bit full adder cells," in Proceedings of the 47th IEEE International Midwest Symposium on Circuits and Systems, pp. 209–212, July 2004.

20. S. Wairya, G. Singh, R. K. Nagaria, S. Tiwari,"Design analysis of XOR (4T) based low voltage CMOS full adder circuit", in Proc. IEEE Nirma Univ. Int. Conf. Eng. (NUICONE), Dec. 2011, pp. 1–7.