Power Optimized High Pass Digital FIR Filter Using LDPC Code

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Abstract

In the many diverse signal processing systems, including control systems, video or audio processing systems, noise - reducing applications, and other telecommunication networks, digital signals play an important role. Due to its spectrum stability and phase shift response, FIR filters are used in this situation. In this paper presents design and implementation of power optimized high pass digital FIR filter using ripple carry adder and radix 4 modified booth algorithm and Low Density Parity Check (LDPC) method is used. Aim of this paper to reducing the errors in transmitted signals using LDPC codes in now days LDPC codes are widely used in 4G and 5G communication. In this paper ripple carry adder and radix 4 modified booth algorithm used to reducing the time delay of the circuit. Comparing our proposed method to existing high pass filter using polar code method. Further the optimization technique is used for filter coefficients optimization after the error correction from the transmitted signals. Design and implement our Verilog code using Xilinx vivado 2020.1 tool and its outputs are verified using simulation tool. Area, Power and Delay are calculated using Xilinx vivado 2020.1 tool.

Keywords— LDPC code, Ripple carry adder, Radix 4 modified booth algorithm, Area, Power, Delay, Xilinx vivado 2020.1 tool

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Introduction

Certain frequencies are undisturbed by the digital filter, whereas others are completely blocked. Infinite Impulse Response filters (IIR) as well as Finite Impulse Response filters (FIR) are different forms of digital filters [1], [2]; which one to choose relies on the respective advantages and uses. FIR filters have an amplitude and phase response, zero phasing distortions, have always been steady, and their output is noise canceling, which is needed in most picture and signal processing applications, interfaces and noise removal, telephone echo cancelation, and signals recovery. FIR filter construction can be done using a variety of ways. FIR filters are frequently designed using the Window technique, however this method wasn't very good at managing frequency response across a broad range of

wavelengths [3], [4]. In information theory, a linear error correcting code, also known as a low-density parity-check (LDPC) code, is a method for transmitting data through a channel with a high probability of being corrupted by noise. Using a sparse Tanner graph as a starting point, an LDPC can be constructed. Due to the fact that LDPC codes are capable of approaching near to their capacity, it is possible to set the noise threshold for a symmetric memoryless channel to be practically close to the theoretical maximum. This is referred to as the Shannon limit. This is achievable because LDPC codes are near-capacity codes. After a certain level of background noise is present, however, it is possible to achieve tolerable levels of data loss. It is possible to decipher LDPC codes in a period of time that is proportional to the length of the blocks of the code when iterative belief propagation methods are used. There is an increasing need for LDPC codes in situations where extremely reliable and efficient data transfer over bandwidth- or return-channel-limited networks is essential, even in the face of corrupting noise. Despite the fact that LDPC codes can be corrupted, this holds true. The available bandwidth of the return channel is one of the constraints that significantly limits these applications. When compared to other codes, especially turbo codes, LDPC codes' practical application has lagged far behind. In a crucial development, turbo codes lost their patent protection on August 29, 2013. LDPC codes are sometimes called Gallager codes after Robert G. Gallager, who introduced the concept of LDPC codes in his 1960 PhD dissertation at the Massachusetts Institute of Technology. The industry standard is Low Density Parity-Check codes. It has also been shown that LDPC codes provide the finest attainable combinatorial characteristics. By adapting the Gilbert–Varshamov bound for linear codes to binary fields [5, 6], Gallager proved that low-density parity-check (LDPC) codes have a good chance of working. You may see an example of Gallager's work [5] here. In 2020, it was shown that Gallager's LDPC codes can perform list decoding and that they satisfy the Gilbert–Varshamov condition for linear codes over general fields. A high-pass filter is the opposite of a low-pass filter, which makes it difficult for signals of a high frequency to get through while letting through signals of a low frequency with little difficulty. Why? Because high-frequency signals are blocked while low-frequency ones travel through relatively unimpeded by a low-pass filter. It may have been obvious from the previous line that low-pass filters are constructed in the opposite way that high-pass filters are. High-pass filters are identical to low-pass filters, except their output voltage exceeds 70.7% of the input voltage at a fixed frequency (the "rated cutoff frequency"). The finite impulse response (FIR) filter is the primary topic of this study [7], [8]. Parameters are used to specify the impulse response of a FIR filter. Digital filters can be further subdivided into a subset known as FIR filters (for "finite impulse response"). The lack of data on their capabilities led to their categorization as analog filters (a recursive part of a filter). Instead of striving for perfection, which is unattainable, this work aims to create filters of a quality that is good enough to be useful. Matlab's FDA tool can be used to create bandpass filters using any of several different FIR design techniques. All filters have the same fundamental frequency and magnitude criteria, but their architectural order is different. Nearing infinity in order, the frequency response of a FIR filter approaches perfection [9, 10]. An accurate linear phase response can be realized with FIR filters. Because of this, we may deduce that the filter does not impart any phase distortion to the input signal. Due to the simplicity of implementation and the continuous demonstration of BIBO stability, FIR filters with bounded input and bounded output (or

BIBO stable filters) find use in a wide range of practical contexts. A FIR filter's filtering tap should be built so that it is symmetrical about the central tap point if linear phase is to be maintained. In this way, the linear phase can be preserved. Moreover, FIR filters are comparatively insensitive to quantum errors in the filter coefficients. Having this quality is crucial in creating effective filters that use digital signal processors (DSPs) or semiconductor-based technologies [11], [12].

What follows is a summary of the remaining parts of the article and their respective organizational structures: Part 2 of this series will focus on some of the most influential studies from the past. In the third portion, many novel algorithms are introduced to provide an in-depth understanding of the work offered here. The success of the implemented plan is assessed in the fourth segment by comparing the outcome to the set criteria. In Section V, we briefly summarize the findings and talk about where the field could go from here.

I. LITERATURE REVIEW

Aakanksha Devrari,Adesh Kumar, Amit Kumar FPGAs were utilized in order to investigate the LDPC and Turbo codes' performance in the communication system. The backbone of the wireless communication system is comprised of multiple coding methods such as turbo codes, LDPC codes, convolutional codes, polar codes, systematic codes, and so on. Both turbo codes and LDPC codes have the ability to provide an error-corrected signal over a noisy channel. Turbo codes have a good coding gain close to Shannon's limit. The LDPC and turbo code encoder and decoder were built with the help of the Xilinix ISE 14.7 software, and the Virtex-5 FPGA served as the target hardware platform for the project. The Xilinx simulation tool is applied in order to ascertain the necessary amounts of space, time, and power for a Virtex-5 FPGA circuit board. Those who are currently working on turbo and LDPC code will find the findings of this study to be quite helpful. Lamjed Touil, Abdelaziz Hamdi, Ismail Gassoumi, and Abdellatif Mtibaa developed a low-power structural FIR filter with signal-driven clock gating and multibit flip-flops. Their paper is titled "Design of Low-Power Structural FIR Filter with Signal-Driven Clock Gating and Multibit Flip-Flops."

In modern digital electronics, FIR circuit is the most essential component of DSP circuit. Power optimization is the most essential in DSP circuit. Signal-driven clock gating (DDCG) and multi-bit flip-flops (MBFFs) are two low-power design methods that are used to optimize the power consumption in DSP circuit. Main objective of the DDCG and MBFF is latches are consuming the power even though latches are rest. This power consumption is reduced using DDCG and MBFF and these results are compared with the existing one. 25% to 22% power consumption is reduced by using the DDCG and MBFF methods. Mohana kannan D.Deepa proposed a design of low power and area efficient FIR filter using modified carry-save accumulator method. In finite impulse response (FIR) filter adder and multiplier circuits are playing a major role and also adder and multiplier circuits are consuming more power and time delay. To overcome these issues modified carry-save accumulator method is used to reduce the time delay and power consumption. Carry save adder and ripple carry adder combine to form the modified carry-save accumulator method. Excising and proposed method outputs are compared with Xilinx ISE 14.5 simulator. In the proposed method area was reduced by 24%, Time delay was reduced by 2%, and power consumption was reduced by 3%. *Hong QIU, Zhaonan Guo, and* Xiangli Zhang design and implement the bandpass

FIR filter with improved distributed algorithm. In bandpass FIR filter adder and multiplier circuits are consume more area and power when compared to the other circuits in FIR filter. To overcome these issues improved distributed algorithm are used. An improved distributed algorithm was used to reduce the binary multiplication and binary adding steps in the band pass FIR filter circuit. Because doing so bandpass filter area and power are reduced with it compared to the existing method. Bandpass filter coefficient values are calculated using FDA tool in MATLAB software. Proposed method results are verified using the Xilinx ISE simulation tool. Sumbal Zahoor and Shahzad Naseem Design and implementation of an efficient FIR digital filter. Nowadays Digital Signal Processing (DSP) circuits are mainly used in the communication field, particularly in aerospace and defense communication. DSP circuit consists of three main modules ADC, Digital filter, and DAC. An interface is needed for ADC and Digital filter. First analog signals are converted using an analog to digital converter (ADC). These converted signals are ready for digital signal processing. Digital filter output back into analog signals using Digital to Analog Converter (DAC). In the proposed method Kaiser Window bandpass filter is used in the Digital FIR filter. Bandpass filter coefficient values are calculated using FDA tool in MATLAB software. The proposed method FIR filter values are compared with the existing FIR filter. Bandpass filter outputs are verified using the Xilinx ISE simulation tool. With it compared to other window methods Kaiser Window method utilize 42% of the area in whole hardware. Debarshi Datta and Himadri Sekhar Dutta designed and implemented the high-performance IIR filter using an FPGA board. In this proposed method FIR based parallel pipeline, method is used to design the IIR filter, and another two methods discussed in the proposed method look ahead and two-level pipeline FIR-based IIR filter. These three methods' outputs are verified using the Xilinx ISE tool. Existing and proposed method outputs are compared. The proposed method IIR filter consumes less power and area with it compared to an existing method. Five inputs two inputs are miss-matched in the other three inputs. The majority of the three inputs' single value is the FMR output. DR.Manoj Kumar, Diamond Singh Soibam implemented the third order low pass digital FIR filter using pipelining retiming technique. Comparing the second-order filter with the third-order filter area consumption, power utilization, and time consumption using broadcast and non-broadcast low pass FIR filter. MATLAB FDA tool are used to calculate the Kaiser window and hamming window coefficient value. Cluster and feed-forward pipelining retiming technique are used to retime the third-order digital FIR filter. Synthesized third-order digital FIR filter values are verified using the XILINX VIVADO simulation tool. Dr.Kiran Agarwal Gupta, Tejashree Patil Implementing the low pass reconfigurable digital FIR filter. Delta-sigma module techniques are used in ADC. ADC output is given to the decimator. Decimator is used to reduce the noise in a received signal. This technique reduces the sampling rate of the received signal automatically adder and multiplier units are reduced. So time consumption decreased by 22% and area consumption decreased by 43.8%. Synthesized FIR filter outputs are verified using the Xilinx Vivado simulator. Jacinta Potsangbam Manoj Kumar proposed combined pipelining and parallel processing techniques are used in IIR and FIR filter. This technique is used to reduce the power consumption, area occupation, and time consumption in Finite impulse response (FIR) and Infinite Impulse Response (IIR). These two filters output values are compared with existing FIR and IIR filter time delay, power, and area values. Synthesized pipelining and

parallel processing FIR and IIR filter outputs are verified using the Xilinx Vivado simulation tool. Dr. Manal H. Jassim, Asaad Hameed Sahar Design and implement the high pass filter using the symmetric method. An FIR filter circuit non-symmetric method is consuming more time delay. This time delay affects the overall device performance. Replacing the non-symmetric method with the symmetric method will consume less time delay when compared to the non-symmetric method. High pass filter coefficient values are calculated using MATLAB software. Non–symmetric and symmetric method outputs are compared and verified using Xilinx simulation tool. Shilpa Thakral, Divya Goswami, Ritu Sharma, Challa Krishna Prasanna Design and implementation of a high-speed digital FIR filter using the unfolding method. Vedic multiplier and carry increment adder is used to reduce the propagation delay of the circuit. This high-speed FIR filter unfolded by a factor of three using unfold factor as thee efficient way to reduce the propagation delay of the circuit. The proposed method results are compared with the existing method. The proposed method propagation delay is three times faster than the existing method. Propose and existing methods are synthesized and their results are verified using the Xilinx ISE tool.

II. PROPOSED WORK

The normalized signal sequence ($N[D_i]$) is fed into the noise filtering phase which is the final phase of the proposed preprocessing unit. In this step, the noise presented in the signal is removed by applying Non-Linear Wiener filter. The wiener filter is the widely used technique for removing noise from the signal set. However, the conventional wiener filter is limited to linear signal and not suitable for processing non-linear signal. Thus, we have used the non-linear extension version of wiener filter for eliminating noises from the signal. The non-linear wiener filter works upon the correntropy which is the function of generalized autocorrelation in the non-linear space. It can be defined as follows,

$$C(t_1, t_2) = E[K(D_i(t_1), D_i(t_2))] \quad (1)$$

Herein, $E[.]$ Represents the expected value operator and K represents the kernel function. Let, $F(D_i)$ be the input of non-linear wiener filter and the composite vector can be built as follows,

$$F(D_i) = [D_i(t), D_i(t-1), .., D_i(t-L-1)]^T \quad (2)$$

Here, L is the length of the filter. The weight values obtained from the filter can be expressed as follows,

$$\Omega = [w_0, w_1, .., w_{L-1}]^T \quad (3)$$

The objective of the filter can be formulated as minimizing the mean square error with respect to the Ω value. From that the filter output ($y(t)$ is given as follows,

$$y(t) = F^T(D_i)\Omega \quad (4)$$

In this manner, the non-linear wiener filter is applied one ach signal sequence in order to extract the input from the noisy signal. The impact of the preprocessing phase is illustrated in figure.3.

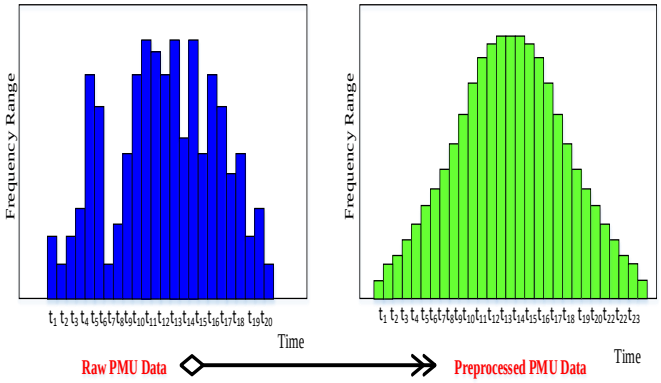

Fig.1. Noise Reduction in Transmitted Signals

The same formula can be used to determine the cutoff frequency of the capacitive high-pass filter, just like it was used to determine the cutoff frequency of the capacitive low-pass filter.

$$f_c = \frac{1}{2\pi RC} \qquad (5)$$

fc is the cutoff frequency

R is the Resistance

C is the Capacitance

High pass filter coefficient values are calculated using MATLAB filter design tool

LDPC (Low Density Parity Check): It is a linear code this code parity bits are calculated using hamming code.

Hamming code formula

2^P≥P+M+1

P – Parity bit

M – Message bit

For example

P = 2

M = 4

4 ≥7 (Incorrect)

P = 4

M = 4

16 ≥ 9 (Correct)

In this paper first three bits are parity bit and last bit are parity check bit.

In hamming code all the parity bits are placed in power two places and remaining places message bits are placed. In this paper four parity bits are calculated using following combinations.

P1 ← 1, 3, 5, 7

P2 ← 2, 3, 6, 7

P3 ← 4, 5, 6, 7

P4 ← 8

1	2	3	4	5	6	7	8
P1	P2	M1	P3	M2	M3	M4	P4

Parity bits are placed in 1,2,4,8 Message bits are placed in 3,5,6,7. For example our message bit is 1011 parity bits are calculated and placed the parity bit position.

1	2	3	4	5	6	7	8
0	1	1	0	0	1	1	0

This is the coded message bit. This 8 bit message are transmitted. Hamming code parity bits are used to calculating the generator matrix. Generator matrix is a combination of identity matrix and parity bit matrix.

$$G = \begin{bmatrix} 1 & 0 & 0 & 0 & 1 & 1 & 0 & 1 \\ 0 & 1 & 0 & 0 & 1 & 0 & 1 & 1 \\ 0 & 0 & 1 & 0 & 0 & 1 & 1 & 1 \\ 0 & 0 & 0 & 1 & 1 & 1 & 1 & 0 \end{bmatrix} \qquad (6)$$

H matrix is combination of Parity bit transpose and Identity matrix

$$P^T = \begin{bmatrix} 1 & 1 & 0 & 1 \\ 1 & 0 & 1 & 1 \\ 0 & 1 & 1 & 1 \\ 1 & 1 & 1 & 0 \end{bmatrix} \qquad (7)$$

$$H = \begin{bmatrix} 1 & 1 & 0 & 1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 1 & 1 & 0 & 1 & 0 & 0 \\ 0 & 1 & 1 & 1 & 0 & 0 & 1 & 0 \\ 1 & 1 & 1 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \qquad (8)$$

H matrix are used to design the tanner graph number of rows called error node and number of columns called message nodes. In H matrix ones are connected the message node and error node combination of message node and error node are called tanner graph.

Tanner Graph: A low-density parity-check (LDPC) algorithm is necessary when sending a message over a noisy transmission channel. Today's electronic telecommunication systems employ forwards error correction (FEC) coding, a group of algorithms, to reduce error in the data transmission across noisy networks. FEC methods are used between wireless network systems, including DSL, cable, and fibre optic. Wireless systems include Wi-Fi, wireless, including satellite communications. A bit (binary digit) is the fundamental building block of knowledge in digital communication, and its value has been most frequently expressed as a 0 or 1. A bit mistake happens when noise (applied electrical disturbances), interfering (from other transmitters), or other causes of distortions causes a broadcast 0 to be interpreted as a 1 and conversely. The average amount of bit errors per unit time is measured by a measure defined as bit error rate (BER) in communication systems. A BER of 10-1, for instance, indicates because one in every ten bits was transmitted incorrectly.

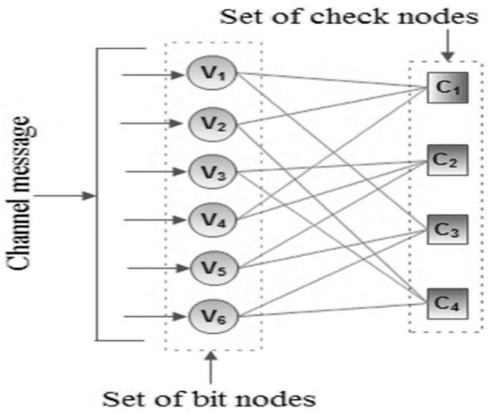

Fig.2. LDPC Outputs

By encrypting the message or increasing redundancies to the bit sequence at the transmitters, FEC attempts to reduce this error rate.

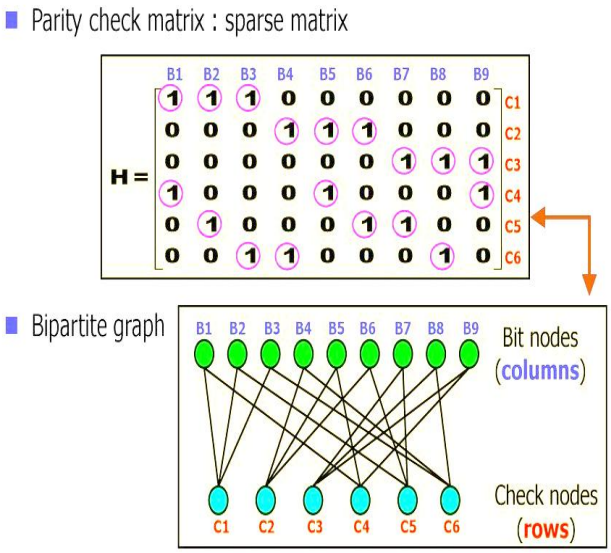

Fig.3. Result for Parity Check Matrix

The equivalent decoder on the receiver side makes use of the additional redundancies to find and/or fix the faults. Repetitive codes, in which a bit is repeated number of iterations, are by far the most fundamental type of coding. For instance, a repetition code with n = 3 converts the input message 011 into the encrypted format 000 111 111. Assume that each of the codewords receives 010 110 101 due to a single bit mistake. 010 is decoded as 0, 110 as 1, and 101 as 1 using a majority voting mechanism by the decoder, producing an error-free received sequence (011). There are various algorithms that offer greater bit error rate while limiting the amount of redundancy, as repeat encoding is quite expensive. Block codes and convolutional codes are the two basic forms of error correction codes. The Viterbi method is typically used to decode convolutional codes, which operate on bitstreams of any length. From the other hand, block ciphers operate on entity's ability that have a predefined size. A very basic type of block coding known as a parity-check code is represented by the parity-check matrix H. A subclass of block codes includes low-density parity-check codes. There are several ways that an LDPC code can be expressed. They can be defined by their generator matrix G & parity-check matrix H, as with any nonlinear block code. Their name comes from

the fact that there are relatively few 1s in their parity-check matrix compared to the quantity of 0s.

According to Tanner's concept, low-density parity-check codes can likewise be graphically depicted (Figure 1). This format aids in describing the decoding procedure and provides a complete presentation of the code. Binary tree graphs are Tanner graphs.

LDPC codes are widely used in 4G and 5G communication system. In wireless communication system bit flips are something that is inevitable to overcome this multi bit flips or burst error LDPC codes are used to correcting the burst error in received bits. In left 1, 2,…..8 are call message nodes and right hand side E1,E2,E3,E4 are called error nodes. All the nodes are connected in the H matrix basis. Increasing the message bit length LDPC code error correcting efficiency all so increased. As a result, the graph's nodes are divided into two separate groups, and its edges only link nodes of the same type. Variation nodes (v-nodes) and checking nodes are the two types of nodes in a Tanner graph (c-nodes). The graph has n variable nodes and m check nodes (the number of parity bits) (the number of bits in a codeword). If the element hij of H is a 1, verify that node fi is connected to variable node cj.

The decoding method for LDPC codes was originally developed multiple times and is known by various names. The belief propagation method, the message-passing method, and the sum-product algorithm are the three most popular ones. The checking and constant nodes exchange messages in order for the decoding algorithms to function. The possibility or "belief" in the "correctness" of the received bit is expressed as a value in these communications. Node c0 sends a message to nodes f1 and f3 in the first phase, node c1 delivers messages to nodes f0 and f1, and so on.

Each checking node fj computes a response to every associated variable node in the second phase. Considering that the other v-nodes connecting to fj are accurate, the response message provides the value that fj considers to be the right one for this v-node ci. In these other words, each c-node fj in the instance is connected to four v-nodes.

In message node first four bits are actual message bits and next three bits are parity bits and eighth bit are parity check bit. Parity check bit are deciding our transmitted bit odd parity or even parity. In this case actual message bits are 10001101 but in some losses in transmitted line third message bit are flipped 0 to 1 our received bits are 10101101. This received bit error are identified and corrected using LDPC code. Error nodes are showing 0111 it means that message node one having two errors, Message node three having Three errors, Message node four having two errors and Message node five having one error. Majority no of error node are connected in third message node. Third message bit are identified and corrected using LDPC code. In case of completion all the steps but still error node shows the errors repeating the hole process until error node errors are cleared.

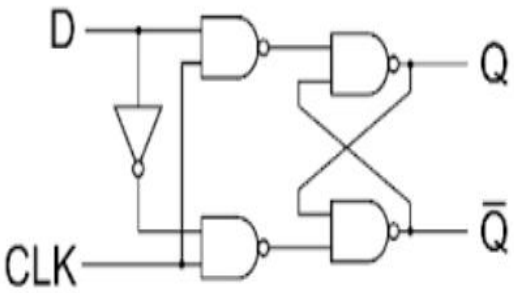

Fig.4. Delay Module

Delay module are more essential then other modules. In FIR filter delay modules are used to delay the ROM output signals because doing so to avoid the setup and hold time violation in FIR filter circuit. In this FIR filter D flip flop as a delay module. D flip flop is transparent flip flop. This D flip flops are mainly used for creating the small delay in circuit. Delay module not used in FIR filter the output values are incorrect or false value.

MODIFIED RADIX – 4 BOOTH ALGORITHM

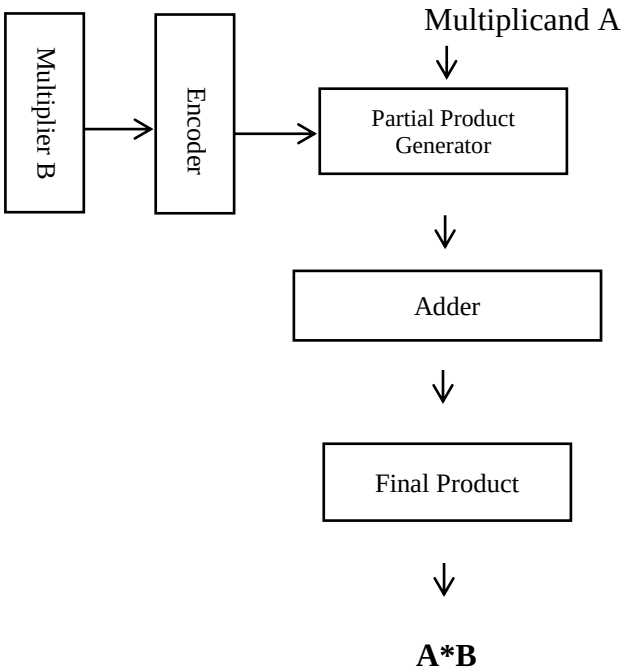

Fig 5. Modified Algorithm

In traditional multiplier consumes more power, area, and time delay. To overcome this problem Modified radix – 4 booth algorithm is used. This algorithm is used to speed up the multiplication time. Radix 4 – booth multiplier is the time delay and area-efficient multiplier it consists of an encoder, decoder, and adder circuit. A full adder is used to add the decoder output. Radix 4 – booth algorithm multiplies both signed and unsigned numbers.

Xn	Xn+1	Xn-1	Recoded Bits	Operation Performed
0	0	0	0	0
0	0	1	+1	+M
0	1	0	+2	+2M
0	1	1	+2	+2M
1	0	0	-2	-2M
1	0	1	-1	-1M
1	1	0	-1	-1M
1	1	1	0	0

Table 1

If 2 even _n‘bit numbers are multiplied, the number of partial products generated is _n/2‘. If _n‘is odd, number of partial products are _n+1/2‘.

Carry Look Head Adder: Carry Look Head Adder compared with ripple carry adder. Ripple carry adder propagation time delay is high. In ripple carry adder output are depending upon the previously generated carry but in Carry Look Head Adder carry only depending upon first full adder output only next carry outputs are generated using another the combination circuit. Advantage of carry look head adder is carry propagation delay is reduced when compared to the ripple carry adder and fast addition logic.

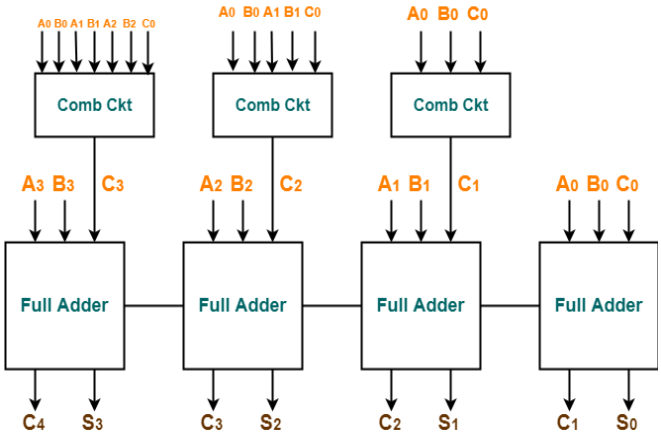

Fig 6 EQUIRIPPLE WINDOW

Simply put, an equiripple filter is one in which each ripple is the same height. Equally high ripples in equiripple filters shouldn't be taken too literally. In order to ensure optimal performance, equiripple filters must be constructed so that the height of these ripples can be adjusted accordingly. It's not just equiripple filters that have this problem.

$$Y[n] = \sum_{K\in 1} h[k]x[n-k] \qquad (9)$$

Where

X[n] – input
Y[n] – output
H[n] – impulse response
I – filter support

$$H\ (e^{jw}) = \sum_{n \in i} h[n]\ e^{-jwn}$$

$$H\ (e^{jw}) = \{-\pi < \omega \leq \pi\}$$

Where

H (e^{jw}) – Frequency response I – filter support

H[n] – Impulse Response

heuristic algorithm that is inspired from the behavior of deer against predators. Primarily, visual power is one of the characteristics which makes the hunting as difficult. In precise, the DHO works on the objective of human to hunt the deer by learning its characteristics. In the proposed work, the objective of the ReDHO is to find the optimal parameters in order to update the SSSC for oscillation mitigation. The algorithm executes the following steps,

Population Initialization: The first step of ReDHO is initialization of hunters as solutions and it can be denoted as the follows,

$$H = \{H_1, H_2, .., H_h\} \qquad 1 < j \leq h \qquad (10)$$

Here, h number of solutions are initialized in the population.

Parameter Initialization: The next important step is to initialize the parameters such as wind angle and deer's position angle. Both angles are important to determine the best positions of the hunters. The search space is considered as a circle and the wind angle is computed as the circumference of the circle as follows,

$$\theta_i = 2\pi rn \qquad (11)$$

Here, rn represents a random number value which is in the range of [0,1] at current iteration i. Similarly, the deer position angle is represented as,

$$\varphi_i = \theta + \pi \qquad (12)$$

On the basis of these equations, the parameters are initialized in the proposed algorithm.

Position Propagation: At the initial point the optimal space is unknown and the candidate solution is considered to be close to the optimum. It can be determined based on the fitness function which is learned by reinforcement learning algorithm. Reinforcement learning agent learns the environment of ReDHO and updates the fitness value of each candidate solution based on oscillation mode, error value, weather and load factors. The fitness is represented as follows,

$$F(i) = \frac{1}{E+L} \qquad (13)$$

The solution which minimizes the error value and load level is selected as the optimal solution under particular oscillation mode and weather condition. This fitness function is the action taken by agent and this policy can be represented as,

$$\pi(F(i), St) = \Pr(F(i)_t = F(i) | St_t = S) \qquad (14)$$

Where, St is the state and the action is the fitness function. For each solution, fitness is determined by learning the reward function which can be given as,

$$R = \sum_{t=0}^{\infty} \gamma^t r_t \quad (15)$$

Here, r_t is the reward at given time t and γ is the discount rate that is in the range [0,1]. By maximizing the reward function, the fitness function is computed for each solution and the candidate with highest $F(i)$ is selected as H^{lead} and the succeeding hunter position is denoted as $H^{succ\,cessor}$.

Propagation through a leader's position: Based on the leader's best position, each candidate in the population attempts to move towards the best position. This process can be modelled as follows,

$$H_{i+1} = H^{lead} - X.p.|U \times H^{lead} - H_i| \quad (16)$$

Here, H_i is the position at current iteration and H_{i+1} is the updated position at next iteration. Also, X, U are the coefficient vectors and p is the random number that represents wind speed and lies between 0 to 2. These vectors are computed as,

$$X = \frac{1}{4}\log\left(i + \frac{1}{i_{max}}\right) b \quad (17)$$

$$U = 2.c \quad (18)$$

The coefficients are computed in terms of maximum iteration (i_{max}), random number (c) in the interval of [0,1] and a parameter b in the interval of [−1,1]. By adjusting the coefficients X and U, the best position H^*, Z^* is updated. For each successful movement of the leader ($p < 1$), all other candidates move their positions. Otherwise, the positions remain as same.

Propagation through position angle: This propagation process enhances the search space by considering the position angle in the update rule. The angle visualization of deer is computed as follows,

$$\delta_i = \frac{\pi}{8} \times rn \quad (19)$$

This visual angle and the wind angle is used to determine a parameter that helps to update the position angle as follows,

$$d_i = \theta_i - \delta_i \quad (20)$$

At last, the position angle at next iteration is computed as follows,

$$\varphi_{i+1} = \varphi_i + d_i \quad (21)$$

The position update is computed from the position angle as given below,

$$H_{i+1} = H^{lead} - p.|\cos(v) \times H^{lead} - H_i| \quad (22)$$

Propagation through the position of the successor: The solution is enriched by the exploration phase in which the U vector is adjusted for position update. In this stage, the position update is performed based on the successor position which results in global search. This update is modelled as follows,

$$H_{i+1} = H^{successor} - X.p.|U \times H^{successor} - H_i| \quad (22)$$

Over iteration, the optimal parameters such as gain block (K), time constants (T_{15}, T_{25}, T_{35} and T_{45}) are optimally determined. Then, the SSSC controller is damped based on these parameters. The following pseudocode explains the process of oscillation mitigation by ReDHO algorithm.

III. EXPERIMENTAL RESULTS

To design low-pass FIR filter for Equiripple window MATLAB FDA tool is used. In MATLAB command window type **fdatool** new window will open depending on your low pass filter specification set the parameters in fdatool window.

Table 2

Properties	Specification
Response type	Low pass
Design method	FIR
Window	Equiripple
Filter order	3rd
Density factor	20
Frequency specification	Normalized 0 to 1
Pass band frequency	0.6
Stop band frequency	0.3
Pass band weight	1
Stop band weight	1

Table 3

Transfer function	Coefficient value
X1	0.1113
X2	0.5102
X3	0.5102
X4	0.1113

Table no 3 X, X2, X3, X4 values are the coefficient value of high pass filter. These four values are obtained by using MatLab filter design tool. These four values are the radix – 4 modified booth algorithm multiplier coefficient value.

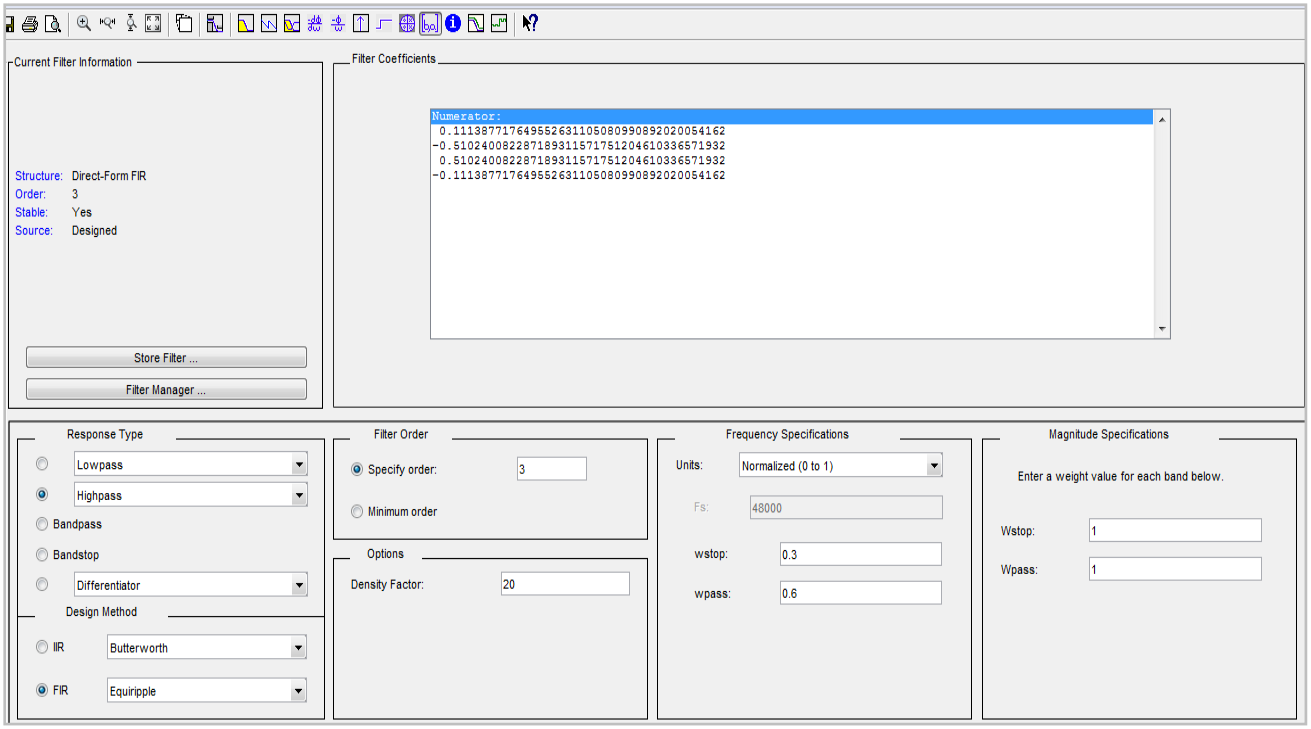

Fig 7 FIR Configurations

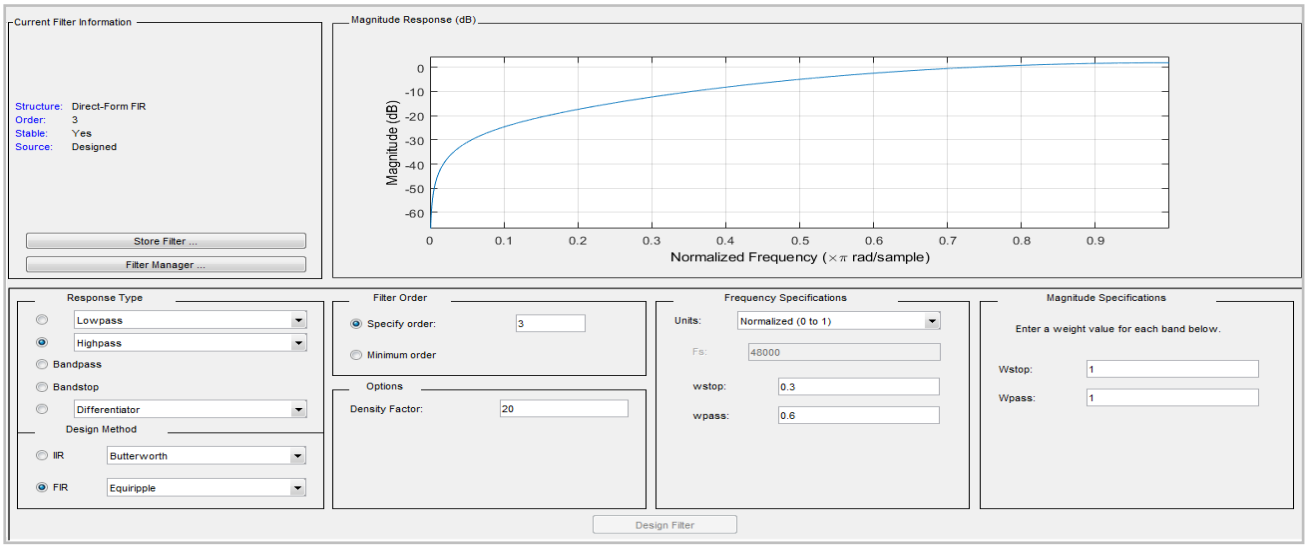

Fig 8 Normalized FIR Filters

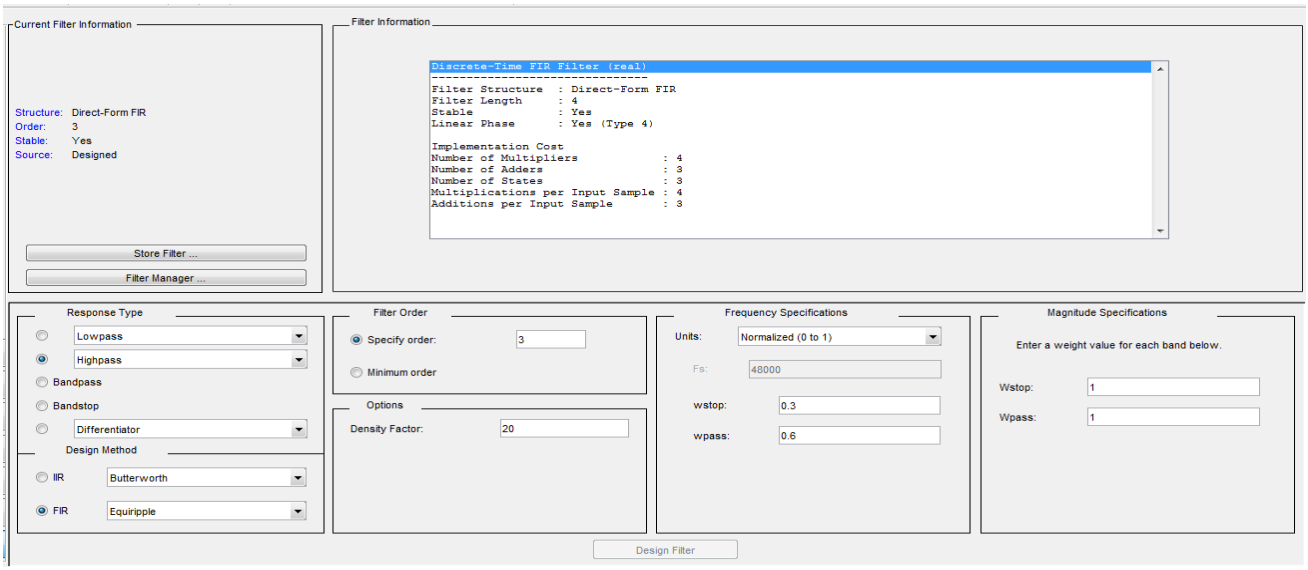

Fig 9 Filter Result

Figure 7 shows that the coefficient value for high pass filter using equiripple window and its stop band and pass band frequency is 0.3 to 0.6. Figure 8 shows that magnitude response of the high pass filter. Magnitude response of the high pass filter is starts from value 1 and end with zero. It shows that frequency increases wave magnitude decrease. Figure no 9 shows that overall information about the high pass filter using equiripple window method. A high pass filter consists of four multipliers, thee adders, thee states, and filter length four.

HIGH PASS FIR FILTER: High pass FIR filter consisting of six main modules ROM, LDPC code, delay, Multiplier, Adder and Output. In this six modules LDPC code module are correcting the errors in received bit. Noised sine wave signals are stored in 160 bit ROM. This sine wave values are given to the delay module it is used to avoid the setup and hold violation in FIR filter output. In this FIR filter radix-4 modified booth algorithm is used to multiplying the ROM and delay module values in this FIR filter carry look head adder is used to adding the present and previous value of the multiplier output. Adder sum value is the final output of FIR filter. Radix-4 modified booth algorithm multiplier coefficient values are calculated using MATLAB filter design tool.

Table 4

Parameter	Existing method	Proposed method
Power	0.083W	0.082W
LUT	55	49
Delay	6.566ns	7.276ns

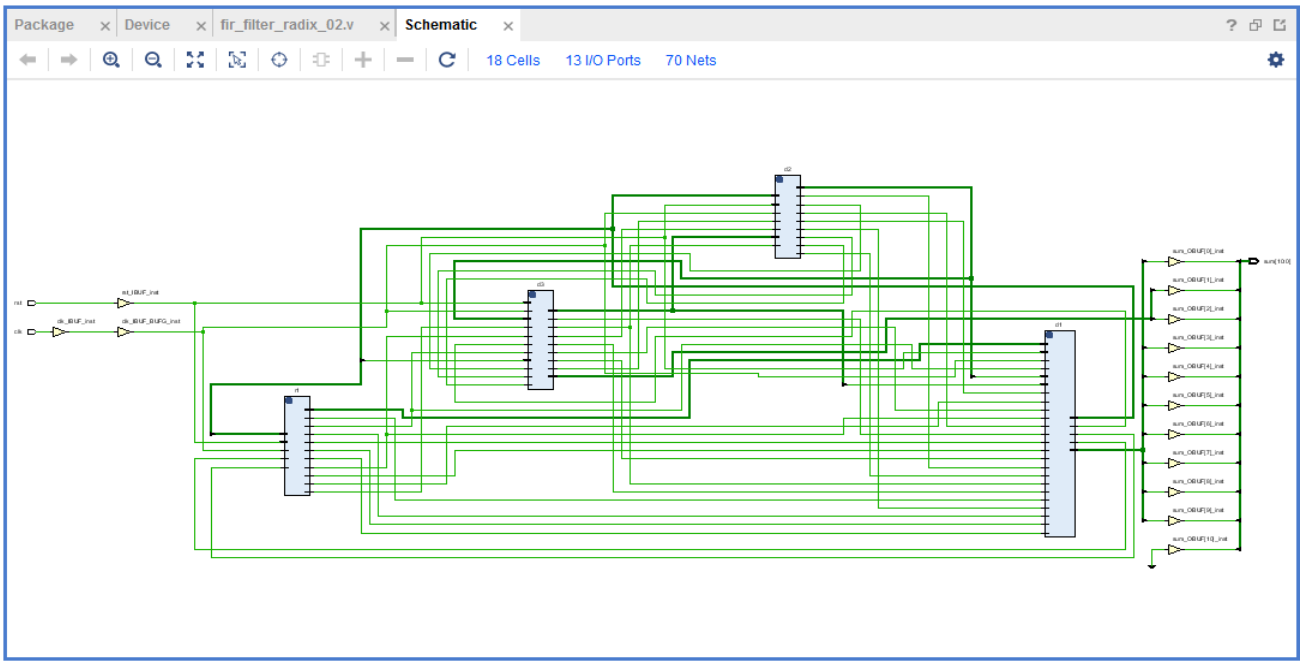

Fig 11 High Pass Filters

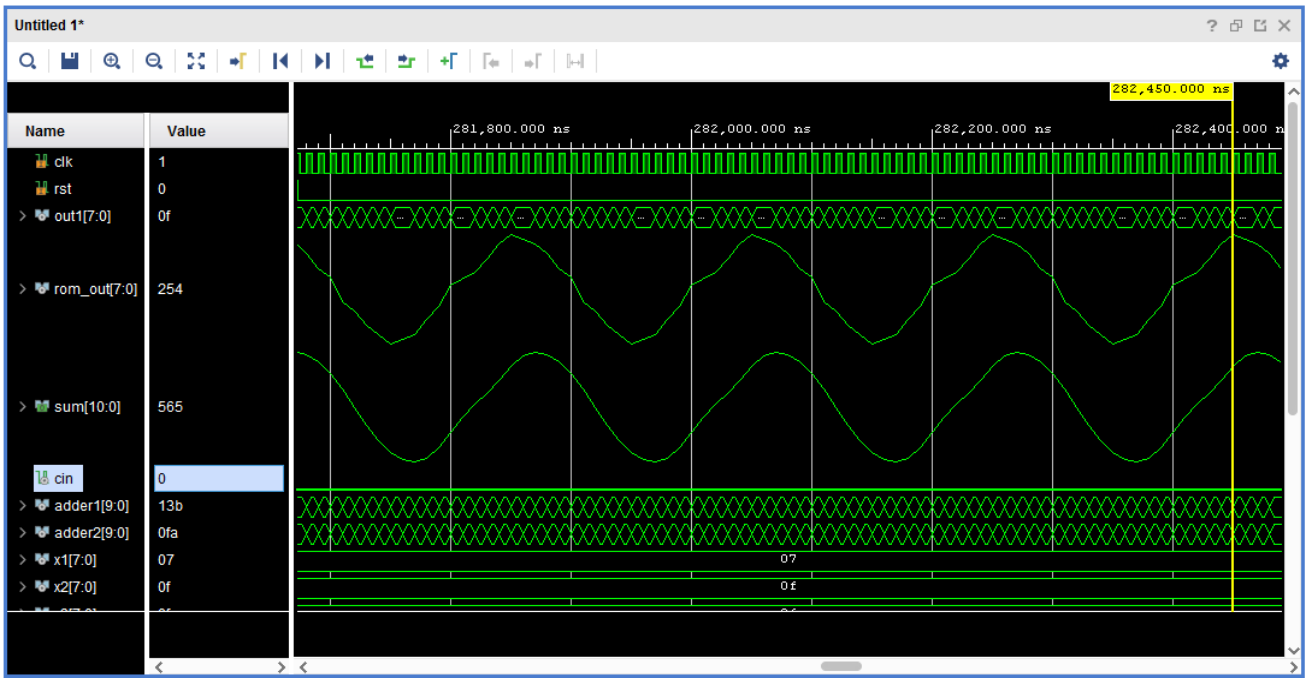

Fig 12 Xilinx Result

This is the overall schematic diagram for LDPC code using FIR filter. In Xilinx simulation tool default wave form output is digital. To select the wave form style in simulation tool digital wave form into analog wave form. The simulation tool digital wave form converted into analog wave form. In low pass FIR filter rom_out is the input and sum is the final output of the low pass FIR filter.

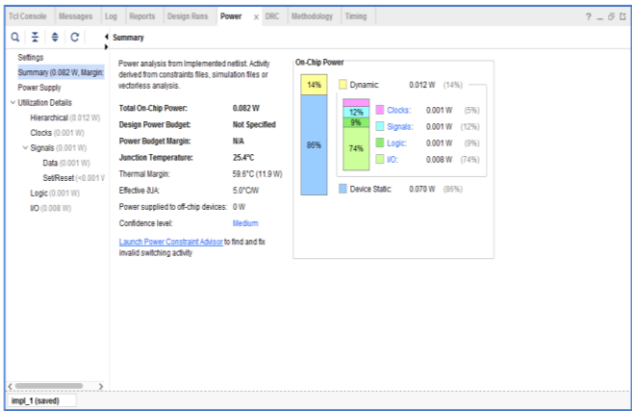

Fig 13 Low Pass Filtering

Figure no. 13 shows that 0.082 W is the overall power utilization on a chip. In this total power report dynamic power are utilize 0.012W and dynamic power utilize 0.070W.

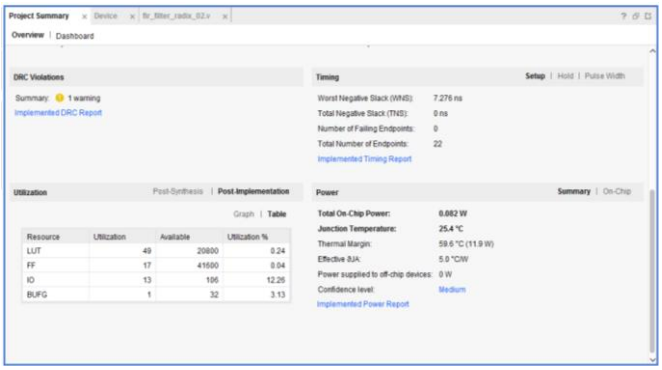

Fig 14 Dynamic Power Results

Figure 14 shows that Low pass FIR filter utilizes 0.24% or 49 LUT of the total chip area and Flip – flop is utilized by 0.04% or 17 of total chip area.

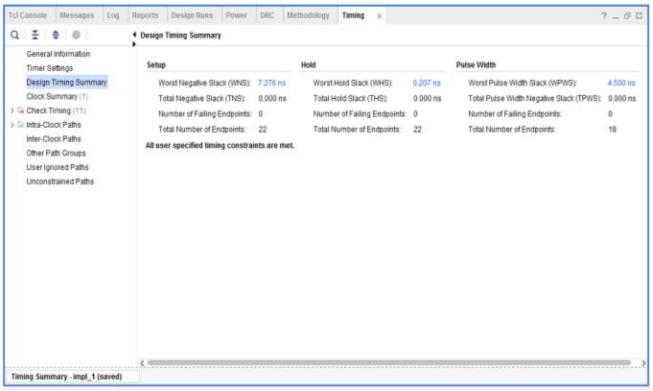

Fig 15 Timing Result

Input must be stable before clock edge is called setup time. The low pass FIR filter setup time is 7.276ns. In case of timing report shows negative value in setup time repeat the same process until positive values are come.

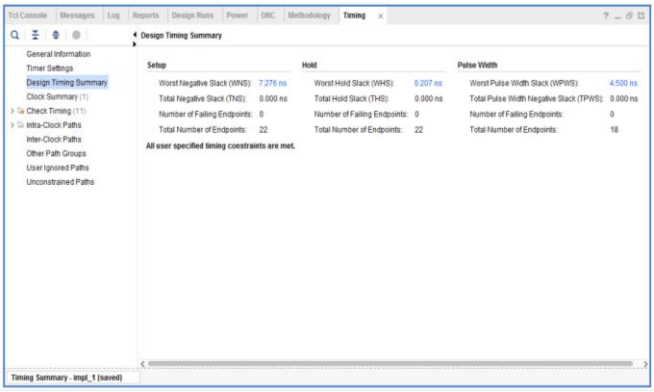

Fig 16 Design Timing Result

Input must be stable after clock edge is called hold time. The low pass FIR filter hold time is 0.207ns. In case of timing report shows negative value in hold time repeat the same process until positive values are come.

V. CONCLUSION

This paper describe the design and implementation of high pass digital FIR filter using Low Density Parity Check (LDPC) code. Digital FIR filter is used to filter the noise in any input signals. LDPC codes are widely used in 5G communication system uses of LDPC code receiver side error rate is minimum when compared to existing polar code. Existing method polar code power, area, and time consumption values are compared to the proposed method power, area, and time consumption values. Existing method values power - 0.083w, area - 55 and time – 6.566ns. proposed method values power – 0.082w, area – 49 and time – 7.276ns. This proposed method Verilog code are design and implemented using Xilinx Vivado 2020.2 and proposed method outputs are verified using Xilinx vivado simulator tool.

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