Content-Addressable Memory (Cam): A Literature Survey

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Abstract

The functional memory which has a large quantity of storage returns the matching data address after comparing the input search data with the data it has already stored.Data is stored, and it is compared to search results using Content Addressable Memory (CAM).Fast access data applications frequently use CAMs. In applications requiring high-speed searching, content addressable memory is used. Pattern recognition, data compression, network security, and Internet router address lookup are just a few applications that extensively utilize CAM. This paper presents a Literature survey on Content addressable memory designing and performance. We are using several methods to design the CAM.Hybrid Memristor-CMOS, NOR type TCAM, Pseudo nMOS Cell andMaster-Slave Match Line (MSML), BiCAM,DG SB-CNTFET are used models in this method.Properties of the CAM are studied for individual methods.Low PowerandHigh Speed Content-addressable Memory(CAM) is very much efficient than other models.

Keywords: Content-Addressable Memory (CAM), Hybrid Memristor-CMOS, High Speed and Low Power, Pipelined Scheme.

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I. INTRODUCTION

Information is stored in a number of memory areas using memory components. If a memory component returns data fast, it is said to be efficient. In traditional memory data is output along with address as the input.In this case, a user must be informed of the address of the location where the data is stored [1].The amount of information makes it challenging to determine the exact location of an address. For this, software-based search techniques are used, eventhoughit takes more time. Content Addressable Memory(CAMs) are

one of the best options for cloud computing applications because of their high speed comparison ability [2]. Applications like pattern recognition, data compression, network security, and address lookup in Internet routers are used in CAMs.The majority of CAM's capabilities are ultimately used by Match-Lines (MLs), which often lookup and compare data [3].

CAM is classified into two types: ternary and binary. And also referred as TCAM and BCAM [4]. In this situation, the BCAM uses both 1's and 0's, whereas the TCAM only uses 1's, 0's, and x [don't care set] [5]. In this paper, we use B-CAM to reduce complexity. Depended on Sparse Clustered

Networks a few associative memories have recently been introduced. One of the key issues is reducing power usage in high capacity CAMs.Simultaneously, when CAM power consumption is exactly proportional to CAM memory size,CAM power consumption should automatically increase when some applications request a larger CAM memory size [6].

The CAM architecture is shown in Figure 1. A CAM is a type of memory component that performs parallel searches and store data in rows. The address where the data was stored is returned if the stored data matches the search data. [7].The Match-Line Sense Amplifier (MLSA)determines whether there is a match or a mismatch.Acommon Match-Line(ML) connects every "C" cell in a wordline. Each matchline ML0, ML1, ML2, and so on is first charged to a voltage level. If there is a mismatch, ML discharges, has a mismatchor else it maintains a high voltage. All matchlines need to be recharged in order to conduct a further search. As a result, ML is frequently fully discharged in content addressable memory [8].

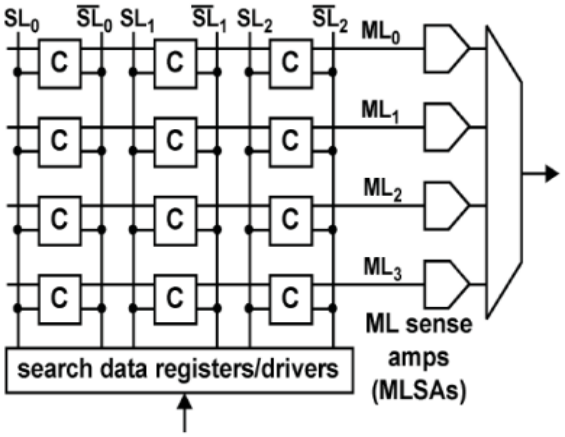

Fig. 1: CONVENTIONAL CAM ARCHITECTURE

The object Gigabit internet asynchronous relocation is a specially constructed circuit count cycle with a high velocity. To use raising edge appliances lower should required to be in a delighted condition.Reverse the huge speed truth tables together with a lesser speed.The elaboration of Content addressable memory architecture is an important challenge. This increased efficiency requires an additional transistor and wiring in each cell. The capability utilization bundle is another issue.The RAM alone is just a part of their Content Addressable Memory where no new cells are accessed as the entire basic is permeate the entire access location.

There are a various type of applications that require quick operations. The employment of CAMs in these applications can be beneficial. However, high-speed network routers where CAM is most commonly used for packet classification and forwarding. The power issue gets worsen when there are more CAM applications and more demand for greater CAM sizes. So the main challenge is to reduce power consumption in large capacity CAMs without sacrificing its speed[9].

In data search applications, CAM outperforms RAM (Random Access Memory).CAM does have some negative economic effects.Each memory bit in a fully parallel CAM includes its own

associated comparison circuit to determine whether the stored bit and the input bit match. This is in contrast to a RAM chip which is made up of simple storage cells. The match outputs of all the cells in the data word must also be merged in order to provide a complete data word match signal. The extra circuitry makes the CAM chip physically larger and more expensive to produce. Every clock cycle activates one of the comparison circuits, which increases extra circuitry in power dissipation. As a result, CAM is primarily used in specialized situations where there is no simpler way to speed up searching.

While CAM&#39:s are mostly used in a variety of applications, including cache controllers for central processing units, memory mapping,coding, data compression and so on. Its primary are used for high-speed network routers and processors that really can fast analyze and forward IP packages.Packet forwarding and packet classification are the two most frequently occurring search-intensive activities carried out through CAMs in routers. The data in the protocol header, such as the destination and source address, outgoing and incoming ports, and other details, is used to establish IP routing. Again store the information in routing tables.The product is delivered to the port(s) mentioned in the table if a match is discovered. The task must be accomplished with large and quick parallelism over extremely fast networks with high traffic volumes. On the other side, big lookup tables and high speeds need silicon area and power consumption.

II. LITERATURE SURVEY

K.Suresh Kumar, R.Manasa Reddy,N.NaveenKumar,et. al. [10] PowerReducing in Content-Addressable Memory Using a nMOSPseudo Cell.The driving phasing recharge is currently designed using Dynamic Content addressable memory. The output circuit was similar during the recharging periodsandmpi transistor is recharging to Vdd. In the valuation phasing output node state,two transistors, mn1 and mn2, coupled to Vss are discharging. As a result, all cycles aside from the matched line are drained by the result charge.It makes use of a vast capability distraction. However, there is an issue with the usage of dynamic circuits in CAM.To charge this result VDD additional recharge and dynamic design need are required. In advance design, the same issues that prevented noising margins are becoming apparent. The design has a heavy burden on clocking. As part of this matching cycle, the Content addressable memory structure charges and discharges m words of Content addressable memory. As a sense amplifier fifth is the need.

Memory with Metal-Oxide Semiconductor Content is identical to the present Content addressable memory word architecture.Furthermore, it completely removes more design released concerns such as noise sharing and charge sharing. Second, there will be no clock signal. As a result, concerns with architecture clocking suchclock skew and clock distribution are having the surplus consideration. Finally it decreases the amount of power used to create this CAM in terms of m word sizes Content Addressable memory

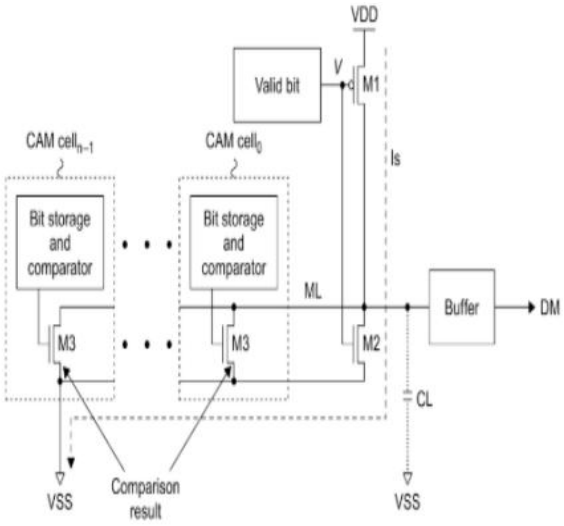

Fig. 2: PSEUDO NMOS CAM DESIGN

The simulation results for the three CAM cells are based on the TSMC 0.25 um CMOS high and 2.5 V of energy. In simulation results, the correct contain addressable memory unit scheduled with different limited bits. With this density movement, the recapture efficiency of these portable memory devices is 200MHz with 32 arguments to another 32 components.These described simulation result displays include addressable memory and take into account the structure's low consumption levels.When compared to the basic contain addressable memory unit and the tenth box of contain addressable memory unit, the effective current-lag that constitutes the scheduled contain addressable memory unit is lowered by more than 45% and 10%, respectively. There are 128 arguments total, each of which is included in the power-delay products and theCAMwas proposed by power-actions.These measured results show how this structure operates at 300 MHz with a reduced passed current of 2.5 V.

Xiaoping Wang, Yuanyuan Yang, Meijia Shang,et. al. [11] presents A Novel Hybrid Memristor-CMOS (Complementary Metal Oxide Semiconductor) Architecture-Based Content Addressable Memory.The author developed a new binary Content Addressable Memory (CAM) design based on 2Memristor and 1Transistor (1T2M) components. The access device is a straightforward transistor, while the memory is made up of two memristors connected in series and holding complementary resistance states in each cell. A two-terminal passive device is a memristor. It is a crucial component of a circuit that specifies how flux and charge interact. Figure 3 displays the CAM cell that this paper introduced.A CAM cell is made up of two memristors (mY and mX) but it has only one transistor (Ms). In addition to storing data as opposing resistances, memristors mY and mX are organized in between series the lines SX/WX and SY/WY. States 0 or 1 are represented by the R_{on} and R_{off} respectively. The datastored logic-1 and logic-0 are represented by the complementary resistances (0, 1) and (1, 0). Transistor *M*s are under the control of line E voltage. In a write operation, *M*sfunctions as both a write path and a discharge path.

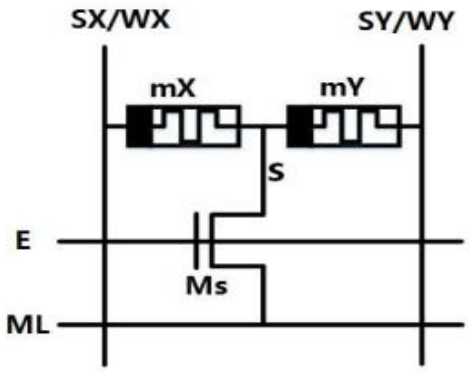

Fig. 3: THE SCHEMATIC OF DESCRIBED CAM CELL

Two phases are necessary in the search process to search the data in a CAM cell. Take the CAM cell in column 0 and row 0 as an illustration. The search voltages are connected to terminals SX_0andSY_0. To terminal E0, an enable voltage is provided. In the first stage, voltage VDD precharges the match lineSX_0(precharge step). In the second phase, if search logic-0, add GND (ground) and VDD (Supply) to terminals SX_0andSY_0, respectively (evaluation step). Nodes S of all cells in a CAM array row are forced to VDD stored data but Match-Line(ML) is not discharged and remains at a high voltage.It only happens whenever the search results coincides with the information present in each CAM cell. When any of the CAM cells do not match the search queries, Match-Line(ML) is discharged to GND and node S is pushed to GND.The frequency of mismatch cells in a rows of the CAM arrays rises as the discharging delays are longer.

In the result analysis, a comparison of the presented 1T2M CAM and the 2T2M CAM is shown. The simulations are performed using Hspice on a single CAM cell. Memristor resistance and transistor pull-down resistance combine to form the equivalent resistance. According to thispaper , the search operation's time delay is the dis-charge period during which the match line's pre-charge voltage falls from 100% to 50%.The number of transistor size, CAM array and mismatch bits word length are only a few variables that can impact the time delay. The presented CAM cell has a less complicated structure than the 2T2M CAM. It has one fewer transistor than the 2T2M CAM cell.Described design can save a significant amount of silicon area compared to 2T2M CAM since transistors require a more space than memristors.Under identical simulation conditions, there are nanosecond delays for both designs, however CAM has the shorter search delay than the described circuit in 2T2M CAM. The given CAM uses less power than the CAM in the 2T2M CAM, which can help in power saving.

Venkata Ramana Datti, P.V. Sridevi, et. al. [12] the Content Addressable Memory Performance Evaluation was explained This paper describes the design of NOR type TCAM (Ternary CAM) and BiCAM(Binary CAM) cells. Figure 4 shows a NOR BiCAM cell. SRAM(Static Random Access Memory) cell is only being required by aBiCAM. When I = 0, a logic "0" is stored, but when I = 1, a logic "1" is stored. Setting SL = 0 and SL| = 1 yields logic "0," while setting SL = 1 yields logic "1." M1 is ON, M2 is OFF, M3 is OFF, and M4 is ON if SL= 0 and I= 0 (the stored and search bits

are the same). Because the matchline is not attached to the ground, ML continues to be high. SL = 0 (the stored and search bits) if I = 1 and SL = 0. ML continues to be high since the matchline is not connected to the ground. M1 is turned off, M2 is turned on, M3 is set on, and M4 is turned off if SL = 1 and I= 0 (the stored and search bits are different). So ML discharges because the matchline is linked to ground.

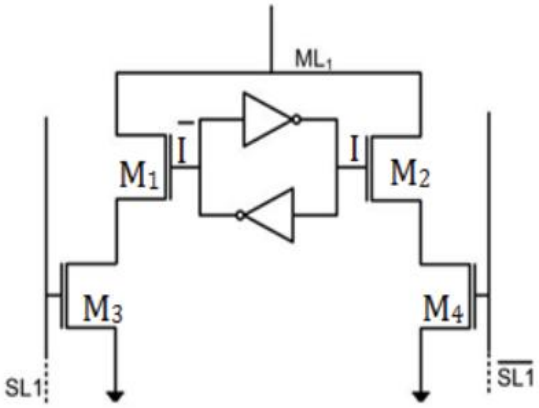

Fig. 4:NOR TYPE BICAM CELL

Compared to BiCAM, TCAM is the CAM that is utilized most commonly. Figure 5 depicts the TCAM cell and its encoding.

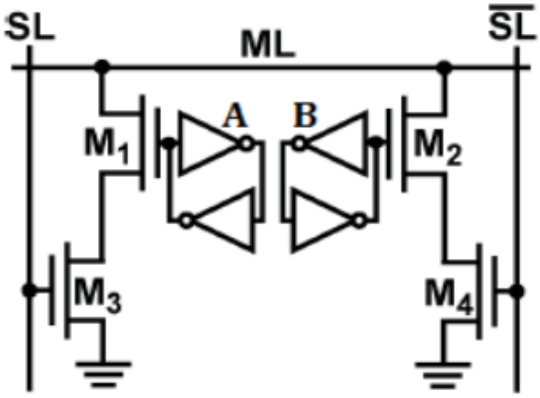

Fig. 5:NOR TYPE TCAM CELL

Two bits needed to define three states using two SRAM cells may be stored in a TCAM cell. Setting B = 1 and A =“0” saves a logic "0" in a TCAM cell, setting B = “0”andA = 1 saves a logic "1," and setting B = 1 and A = 1 saves don't care(X). B= “0” and A= “0” here stand for an unoccupied state. Setting SL = “0” and SL| = 1 looks for a logic "0" in a TCAM cell, settingSL|= “0” andSL = 1 looks for a logic "1," and setting SL = 1 and SL|= 1 searches for don't care(X).

The Ternary and Binary With the help of Cadence 45nm technology, CAM cells were produced. The BiCAM cell uses 12.4W on average as power consumption of the BiCAM cell is 12.4W, while that of the TCAM cell is 14.9W, as seen by the waveforms. 20% more power is used by TCAM

cells than by BiCAM cells. TCAM cells also have the benefit of being simple to keep in three states. TCAM cells have more surface area than BiCAM cells on both sides.

Pasula Ramakrishna, S.Rajendar, Nagarjuna Malladhi, et. al. [13] research indicates an unique low power Master-Slave Match Line (MSML) design for memory architectures based on 4T Content Addressable Memory (CAM) cells. The master-slave architecture and charge refill reduction techniques are the basis of the MSML design.This lowers the ML's supply voltage and power consumption. The matching line is separated into Slave Match-Lines in the MSML architecture (SMLs) and Master Match-Lines (MMLs).During search activities, charge is shared between SMLs and MML to reduce the charge refill in MML.Figure 6 shows an MSML architecture with 'N' SMLs and 4T CAM cells.With charge keeper the search result is shown through the Final Match-Line (FML).

The FML & MMLwill similarly go high during the pre-charge stage, if the PRE signal is high, but all SMLs will fall low. Since search data has yet to be loaded onto search lines, bit lines are reset to "0" during this phase. "0" is the output of the comparison unit to logic. The pull-down transistor is disabled as a result of these findings, preventing the MML charge from accessing the SMLs.When the PRE signal is "0" during the match assessment phase, the search lines are placed by search data. This step checks search results with data that has been stored. Match and mismatch conditions are two situations that occurs.

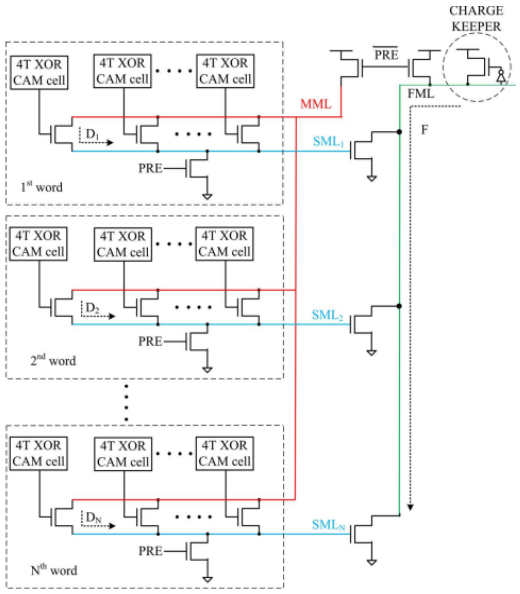

Fig. 6: MSML DESIGN WITH 4T CAM CELLS AND N NUMBER OF SMLS

In MSML design the remaining voltage in MML after the search process is used to establish the final balancing voltage. As mismatch SMLs are improvedthe voltage of final balance is reduces. A significant amount of voltage is needed because the search operation needs the entire power supply. The MSML architecture's final balance voltage helps to solve this problem. Every time itperforms out a significant number of search operations, itdon't have to provide ML with the entire supply.

Thevoltageof final balancing can be reduced by 40%–60% in MSML design throughout the search process.

In comparison to standard CAM design, MSML design uses less ML power.The quantity of mismatch SMLs causes an increase in the ML energy usage in MSML designs. When 6T CAM cell compared by MSML architecture, MSML design with 4T CAM cell utilizes less average electricity. Match design grows along with the number of mismatch SMLs. MSML design with 6T CAM cell uses two transistors for search operations and four transistors for information storage. Two transistors are used for data storage in the MSML architecture with a 4T CAM cell, and two transistors are used for search operations. Between both the MSML design using a 4T CAM cell and the MSML design utilizing a 6T CAM cell, this resulted in a 25% space reduction. When compared to MSML devices with 6T CAM cells, MSML designs with 4T CAM cells lower power consumption by 62%, area by 25%, and delay by 11%-30%.
Debaprasad Das, HafizurRahaman,Subhajit Daset. al. [14]uses a Dual Gate (DG) Schottky-Barrier Carbon Nanotube Field Effect Transistor to demonstrate how to construct and analyse a fast, 11-transistor Content Addressable Memory (CAM) unit (SB-CNTFET). An 11-transistor elevated CAM cell configuration is shown in Figure 7. The basic 8T-SRAM cell architecture uses the M1M8 transistors for data read and write operations. A data search circuit is also presented to be developed using M9M11 transistors.

Data of complementary is delivered into the CAM device using data lines throughout write operations in low power, super fast CAM cells (DL (Data Line) and DLB (Data Line complement)). The M5 and M6 transistor returned on when theline of Write Enable (WE) is reduced to a minimum, bringing the voltage level of node A and B to a similar stage as the data line. The supplementary selected data lines, DL and DLB, are components that contribute to VDD.Pulled up before read operation, the Write Enable line (WE) is activated, disabling the M5 and M6 transistors and preventing any new information from entering the CAM cell.The data stored (A) is accessible at the Reading Data Line (RDL) through to the Bit Line (BL) when the read enable line (RE) is pulled low. Only when the transistor M7 is turned on via the read enable (RE) line will the information from the bit line be accessible in the read data line (RDL).

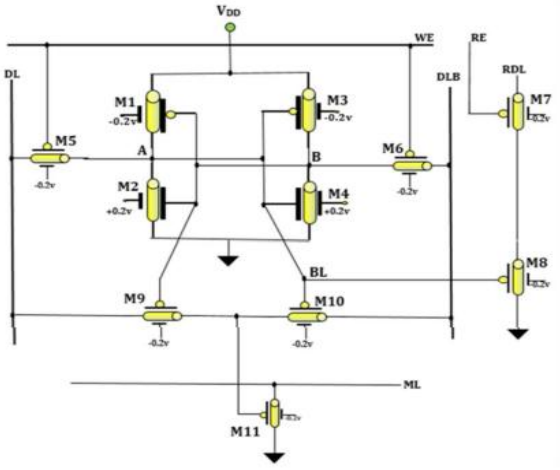

Fig.7: DG SB-CNTFET BASED 11-TRANSISTOR LOW VOLTAGE CAM CELL

Prior to the search procedure the Match-Line (ML) is pre-charged to VDD. If the search results and the stored data do not match the match line is formed when "data to be searched" is placed into the data lines (DL and DLB). Otherwise the match line remains logic high suggesting that the stored and search data were equivalent. The match line will remain high, indicating a match, for instance, if "data to be searched" is stored in data lines such as DLB="0" and DL="1" and the CAM cell storage unit displays B=0 and A="1". Transistors M9 will be ON at this time, whereas M11 and M10 will be OFF. The match line would remain high (ML| = 0) since no conducting path to ground could be found. When the "data to be searched" is entered with DLB=1 and DL=0, the match line alternatively becomes low to indicate a mismatch. Transistors M10 and M11 are turned ON in this instance whereas M9 is set to OFF. Once the match line successfully creates a conducting path to the earth, it is down to low (ML| =1). The address of the n-bit CAM cell can be found using this match line.

We took into account the delaypower, and Power Delay Product (PDP) for cells of CAM developed to use a Verilog-AMS (Analog and Mixed Signal extensions)-based controller suitable model of the DG SB-CNTFET and designed extensively to simulate in the Spectre® Cadence® simulator in the environment of Virtuoso®in order to measure the effectiveness of the low power, DG SB-CNTFET 11T CAM cell fast speed. This design is capable of running on a voltage level of just 0.5 V. A Si-32 nm Technology node of MOSFET (Metal-Oxide Semiconductor Field-Effect Transistor) CAM cell produced at 120-times power delay than an SB-CNTFET. The power-delay ratio of the M-CNTFET based CAM cell is three times higher than that of the SB-CNTFET. The DG SB-CNTFET based CAM cell's power delay product (falltime metric power = PDP) is 407 and 2 less than that of the Si-MOSFET based and M-CNTFET based designs, respectively.

III. COMPARATIVE ANALYSIS

Table 1: COMPARATIVE ANALYSIS

Authors	Model used	Performance parameter
K.Suresh Kumar, N.Naveen Kumar R.Manasa Reddy	pseudo nMOS Cell	power-delay product (PDP)
Xiaoping Wang, Yuanyuan Yang, Meijia Shang	Hybrid Memristor-CMOS	Supply voltage, transistors count, search delay
Venkata Ramana Datti, P.V. Sridevi	NOR type TCAM and BiCAM	average power consumption
Pasula Ramakrishna,	Master-Slave	Power consumption,

S.Rajendar, Nagarjuna Malladhi	Match Line (MSML)	mismatch delay, Area, delay
Debaprasad Das, HafizurRahaman, Subhajit Das	DG SB-CNTFET	Delay, power, power-delay product (PDP)

IV. CONCLUSION

In this paper, A literature survey on Content Addressable Memory (CAM) designing is described.Over traditional memories,Content addressable memories has many advantages. Different models are used in designing of Content Addressable Memory elements. PseudonMOS Cell, Hybrid Memristor-CMOS, NOR type TCAM and BiCAM, Master-Slave Match Line (MSML) and DG SB-CNTFETare used technologies in this method.CAM cells with tiny, high-speed,low-power stable memory circuits can be used in future VLSI circuits that require high-performance store and search operations.

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