Design of SRAM Cell with Sense and Precharge Amplifiers

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Abstract
In this work the design of SRAM cell using precharge and sense amplifier is proposed. , Embedded SRAM units have become an important block in modern SOC's. With the rapid growth of transistor count in the SRAM units, the SRAM unit is a power hungry block from both dynamic and static perspectives. One way to design a SRAM cell is to use sense and precharge amplifiers. The sense amplifier is used to read the data stored in the cell, and the precharge amplifier is used to set the initial state of the cell before a read or write operation. The precharge amplifier is activated, which sets the output of the SRAM cell to a known initial state either 0 or 1. The sense amplifier is activated, and it compares the output of the cell with the initial state. If the output has changed, it means that the data stored in the cell has been modified. The sense amplifier amplifies this small change in output, making it easier to detect. Based on the output of the sense amplifier, the data stored in the cell can be determined. If the output of the sense amplifier indicates that the data has not changed, the data stored in the cell is the same as the initial state. If the output of the sense amplifier indicates that the data has changed, the data stored in the cell is the opposite of the initial state. After the read operation is complete, the sense amplifier is deactivated and the precharge amplifier is reactivated, setting the output of the SRAM cell back to the initial state. Overall, the power consumption of a SRAM cell with sense and precharge amplifiers will depend on a variety of factors, including the specific design of the cell and the operating conditions. It is generally considered that SRAM cells are more suitable for applications where low latency and fast access times are more important than power efficiency, whereas DRAM cells are more suitable for applications where power efficiency is a primary concern.

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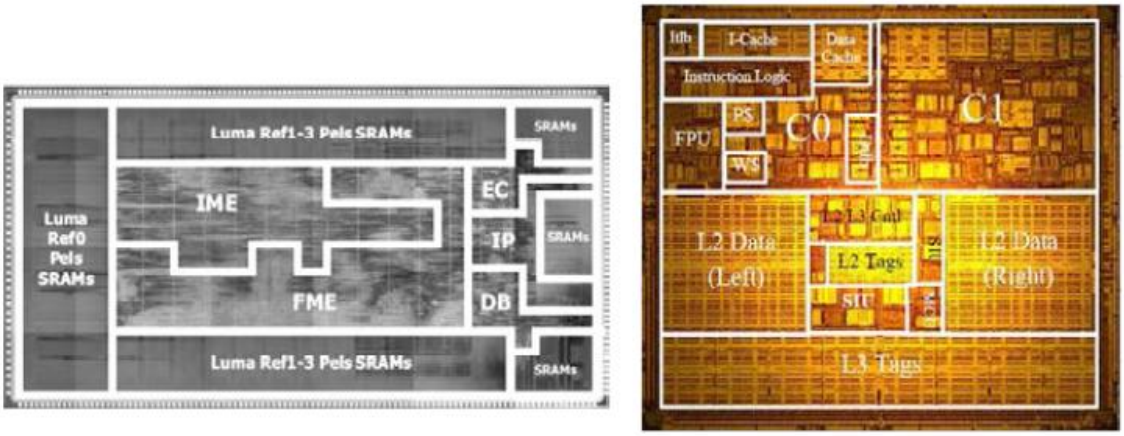
I. Introduction

A SRAM cell is typically composed of 6 transistors and is used to store a single bit of data. The cell consists of two cross-coupled inverters, with each inverter having two transistors. The two transistors in each inverter are typically referred to as the "pull-up" and "pull-down" transistors. The SRAM cell also has two access transistors, which are used to access the stored data. The access transistors are controlled by a pair of bit lines, one for each inverter.

To read the data stored in the SRAM cell, the access transistors are turned on by applying a high voltage to the control gates of the transistors. This allows current to flow through the transistors and

the stored data is read from the bit lines. To write data to the SRAM cell, the access transistors are turned on and the data is written to the cell by applying the appropriate voltage to the bit lines. The sense and precharge amplifier is used to amplify the small differential voltage between the bit lines and to precharge the bit lines to a known voltage prior to a read operation. This helps to improve the reliability and speed of the SRAM cell. A Static Random Access Memory cell is a type of memory that stores a single bit of data. It consists of a pair of complementary metal-oxide-semiconductor (CMOS) inverters that are connected together in a latch configuration. The data is stored in the state of the latch, with one inverter holding a logic "0" and the other inverter holding a logic "1". To access the data stored in a SRAM cell, a sense amplifier is used to read the data and a precharge amplifier is used to set the initial state of the latch. The sense amplifier is a high-gain differential amplifier that is used to detect the small voltage differences between the two inverters. The precharge amplifier is used to apply a strong precharge voltage to the inverters, which sets the initial state of the latch and ensures that the sense amplifier can accurately read the data. To read the data stored in a SRAM cell, the sense amplifier is activated and the voltage difference between the two inverters is amplified. The amplified signal is then used to determine the state of the latch, and the data is output accordingly. To write new data to the SRAM cell, the precharge amplifier is activated to set the initial state of the latch, and then the data is written to the cell by activating the appropriate inverter. Embedded SRAMs are the prominent embedded memories used in today's SoCs. SRAM's integrability with standard CMOS technology gives it an ample opportunity to become the highest area consumer of many SoCs ranging from a high performance server processor to a an HDTV video processor as shown in Figure. 1. Unlike DRAMs, SRAMs do not require data refreshing mechanism. This is because an SRAM cell can store the data indefinitely as long as it is powered. This feature saves the complex and the area consuming data refreshing periphery circuits and makes medium size SRAM units a feasible choice for implementation in the standard CMOS process.



(a) (b)

Figure 1: (a) A Video processor and (b) a Sparc processor.

II. Literature Survey

Many researchers have suggested a numbers of the techniques for SRAM cell design. A brief evaluation of a few significant Static RAM cell designs is existing in this part. Byung-Do Yang [1] proposed a small power Static RAM using BL accuse recycle for understand writing and put in writing operations. This proposed charge recycling SRAM design was based on the hierarchical BL architecture and BL charge recycling method. The proposed method was achieved less degradation of SNM, 17% & 84% of read and write power consumption respectively achieved. other than the operation speed is inadequate to 145MHz.W. Kang et al. [2] introduced a non-volatile SRAM propose with Magnetic Tunnel Junction. They designed MAP of the MTJ device. The switching techniques provided better accumulate power, delay, and dependability disquiet. The main limitation of the system is, it consumes more switching power. A. Makosiejet al. [3] introduced TFET-based 8T SRAM cell. The 8T SRAM cell maintains full functionality in all operation modes at 1V supply voltage with no architectural limitation linked to the half-selection problem. The cell design allowed the use of long word lines with bit interleaving. The major drawback of the Static-RAM design is, whenever the supply voltage increases, at the time substantial leakage power also increases. E. Karl et al. [4] proposed a huge presentation, voltage scaling of 162 Mb Static RAM range was urbanized in 22nanometer tri-gate bulkiness equipment. The 22 nm tri-gate technology delivered a 0.092m High-Density Cell (H-DC) bit cell and 0.108 m Low Voltage Cell (LVC)bit cell. The main limitation of the 6TStatic-RAM design is, internal sensing delay is very high. These all related works have several issues like more delay and power consumption, high critical cell design. Here, the 6T-SRAM-AAM cell design is implemented to overcome these problems and to minimize dissipation of power and delay comparasion of existing SRAM cells design. To reduce the power requirement for charging/discharging in the 7T- SRAM circuit a single BL is used [5]. The low down power SRAM circuits contain develop into a important component of many VLSI circuit chips [6-8].In past decades, the traditional CMOS technology has been affected by two major problems, those are less reliability and more power utilization [9]. Through a write down operation,60% of the total dynamic power require to operate bit lines in traditional SRAM cell designs [10].

III. Implementation

It is noteworthy that SRAMs are widely used in many other applications such as cache memories of multi-purpose processors. SRAM is going to take more than 60% of the SoCs in a near future. As the technology scales, the density of the transistors in the SRAM units increases substantially. The demands for power reduction of the SRAM units have compelled many researchers toward innovative low-power circuits. Six transistors has been widely recognized as a suitable choice for low-power applications. Figure 2 depicts a regular 6 transistor SRAM cell which holds one bit of data in an SRAM unit. It generally consists of a loop of two inverters and two access transistors. The NMOS transistors M3 and M4 are called drive transistors and are responsible for discharging the bitline during the read operation. Transistors M2 and M1 are referred to as access transistors. Once active they allow the internal nodes of the cell(i.e., node A and B) to communicate with the bitlines. The gate of the access transistors is called wordline (WL). The PMOS transistors of M5

and M6 are called load transistors. Depending on the logic value stored in the cell, one of the internal nodes of the cell is at VDD and the other one is at VSS.

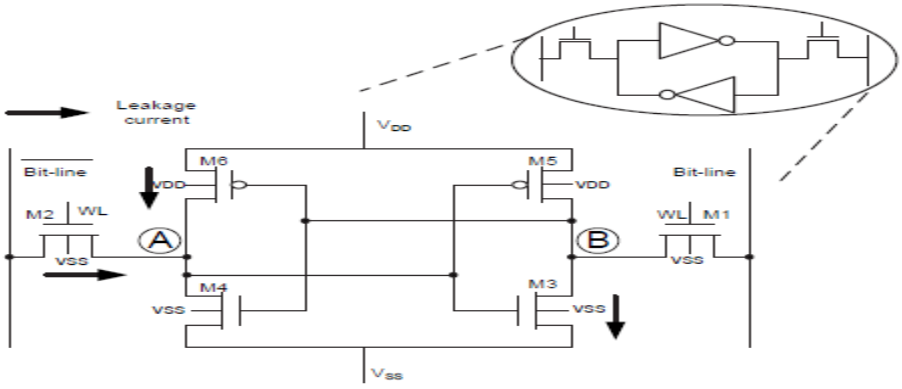


Figure 2: An SRAM cell

Memory cells are the key components of any SRAM unit. An SRAM cell can store one bit of data. An SRAM cell comprises two back-to-back connected inverters forming a latch and two access transistors. Access transistors serve for read and write access to the cell.
Figure 3 and 4 depicts the basic read and write operations of SRAM cell with their models.

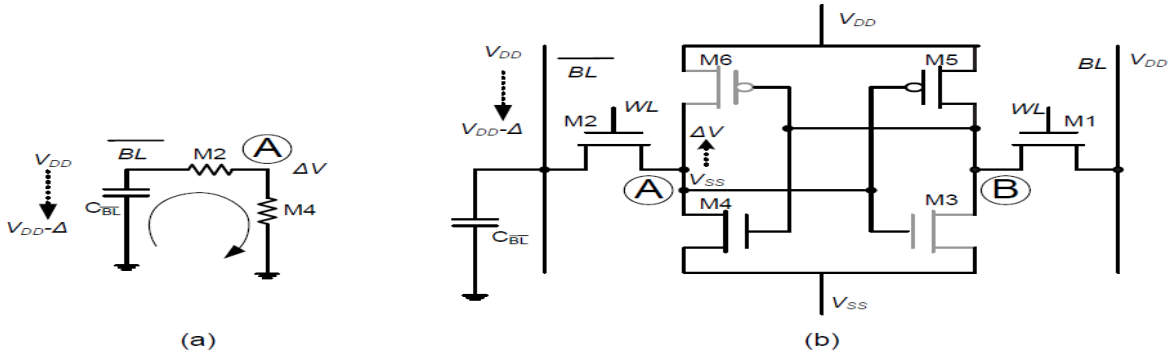


Figure 3: An SRAM cell during read operation: (a) linear model of transistors involved in bitline discharge (b) cell status during read operation.

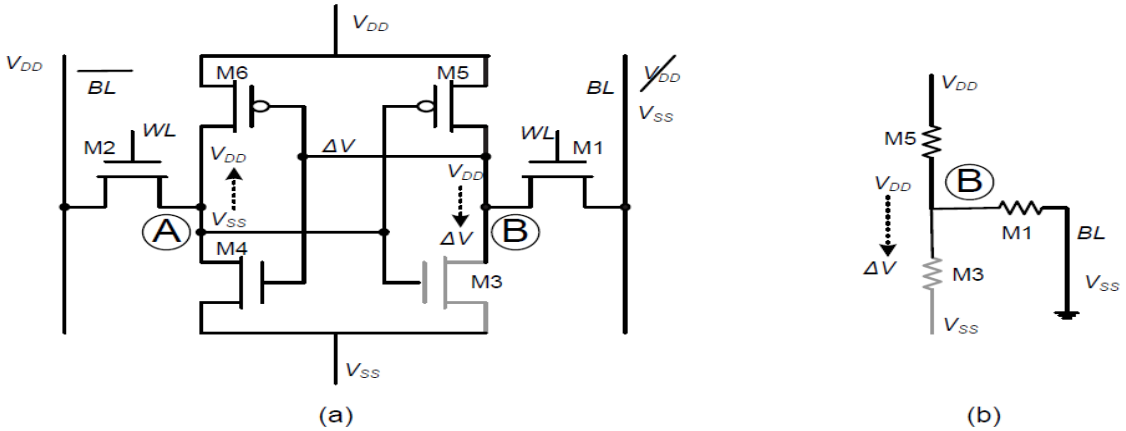


Figure 4: An SRAM cell during write operation:(a) linear model of transistors that initiate the write operation (b) cell status during write operation.

RAM cells are known for their fast access times and low latency, but they also have higher power consumption compared to other types of memory, such as DRAM Dynamic Random Access Memory. In terms of static power consumption, SRAM cells use more power than DRAM cells because they need to maintain their stored data even when the power is turned off. This is because SRAM cells use multiple transistors to store each bit of data, whereas DRAM cells use a single capacitor to store each bit. In terms of dynamic power consumption, SRAM cells also tend to use more power than DRAM cells because they require more transistors to perform read and write operations. However, the difference in dynamic power consumption between SRAM and DRAM is not as significant as the difference in static power consumption.

IV. Simulation Results

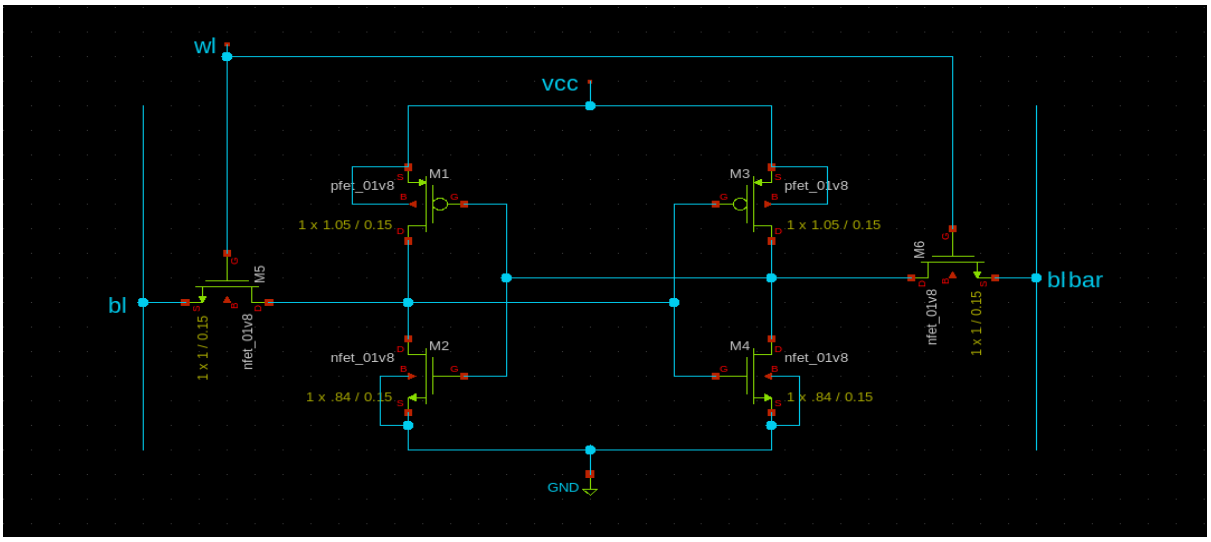


Figure 5: 6T SRAM CELL.

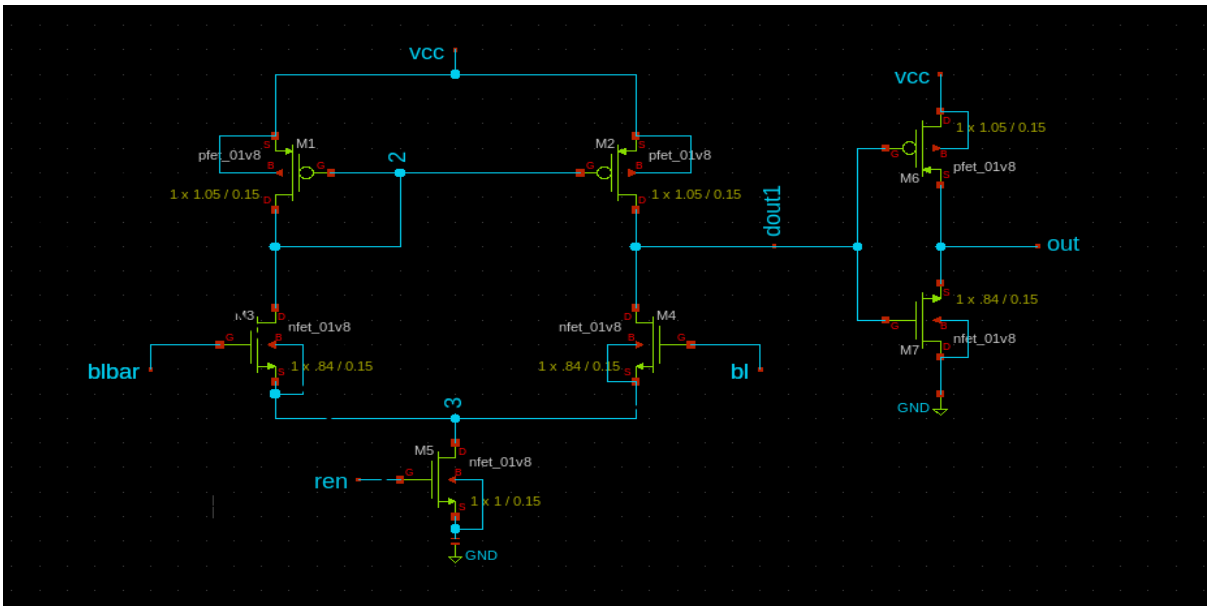


Figure 6: Differential Sense amplifier.

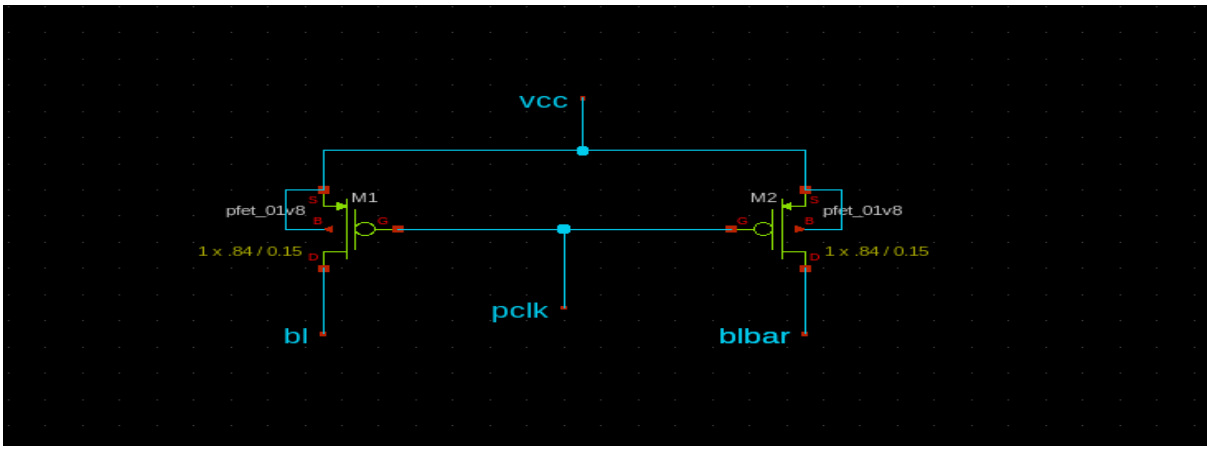


Figure 7: Sense Amplifier.

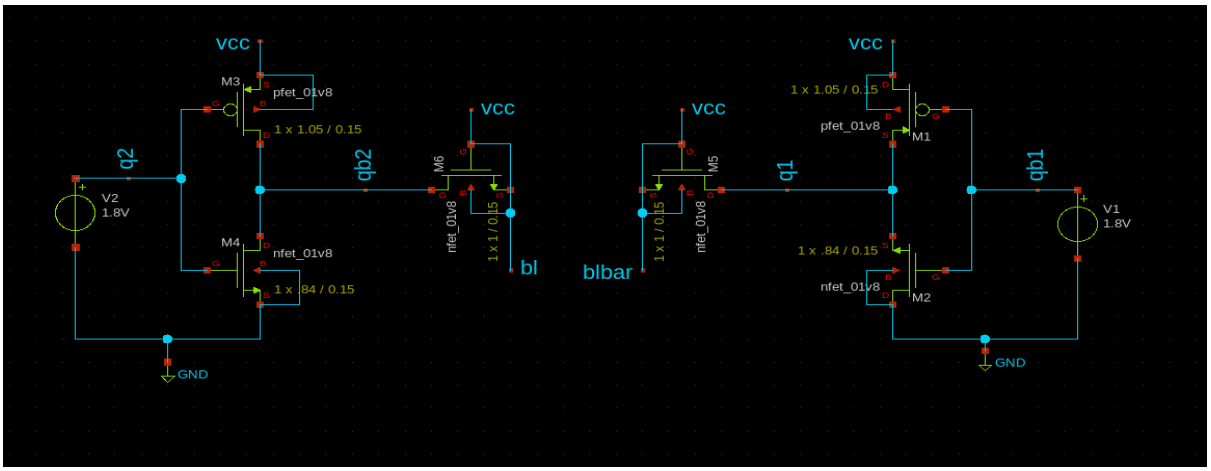


Figure 8: Read Operation.

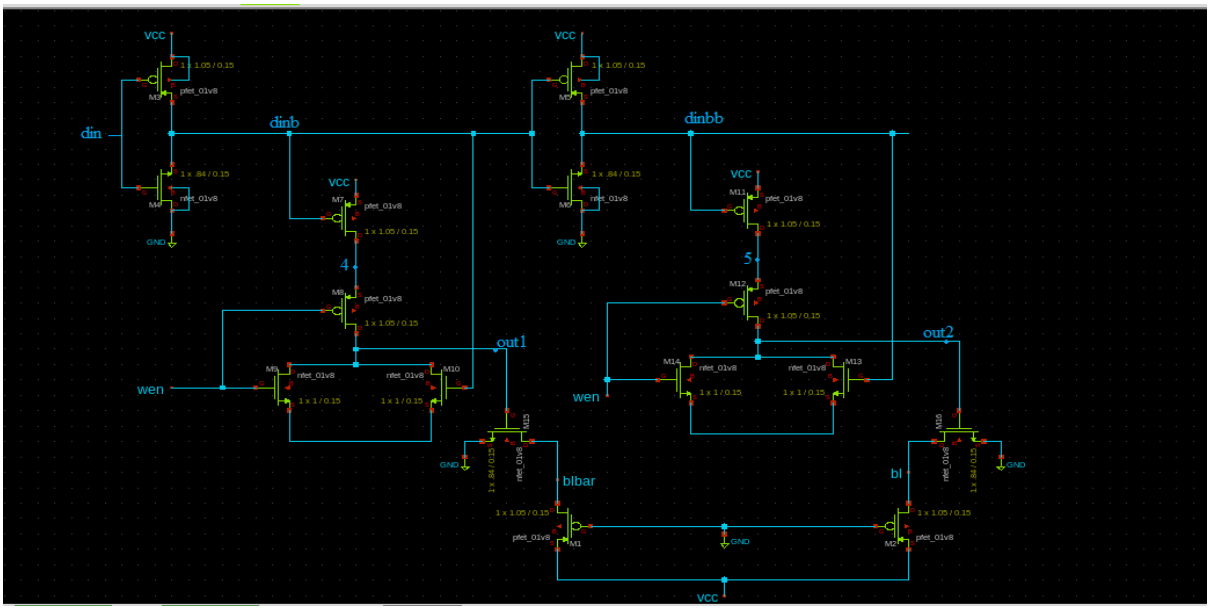


Figure 9: Write Operation.

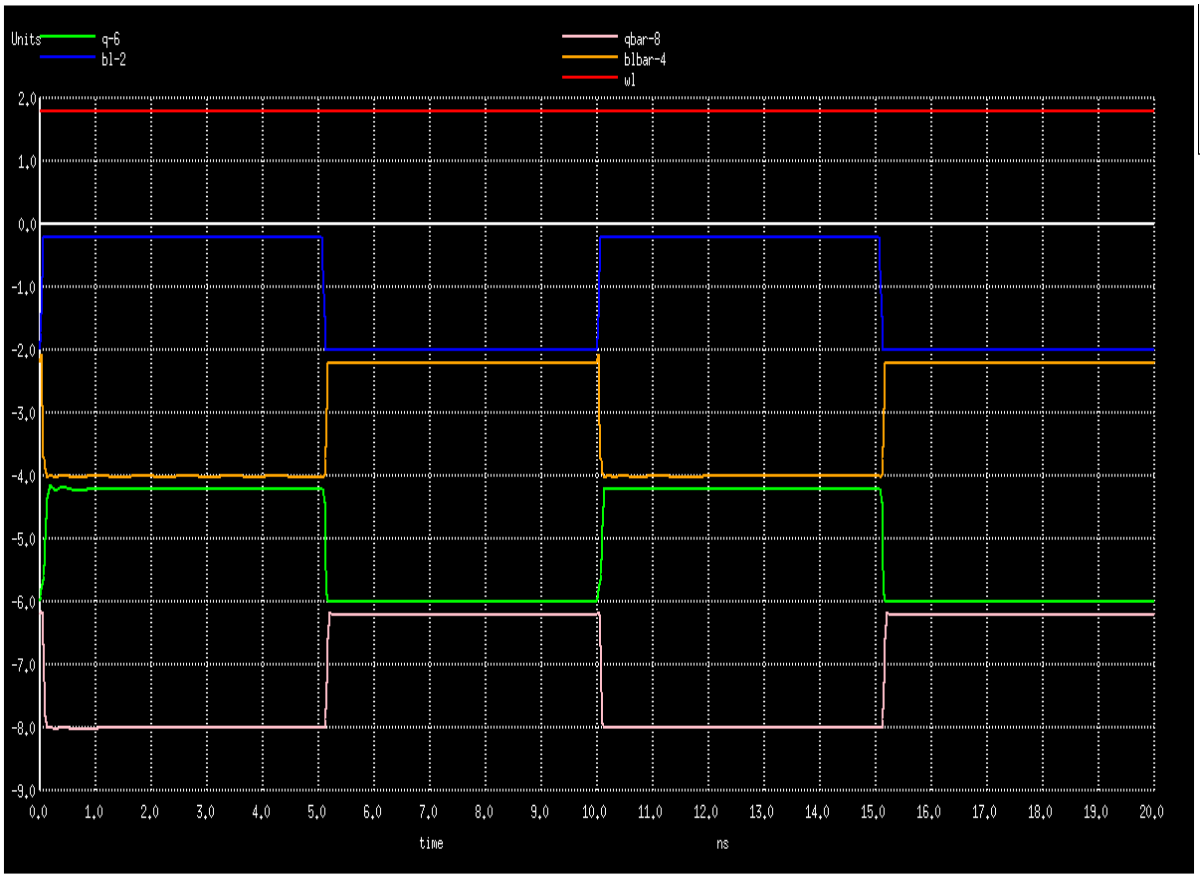


Figure 10: timing diagram of 6T Cell.

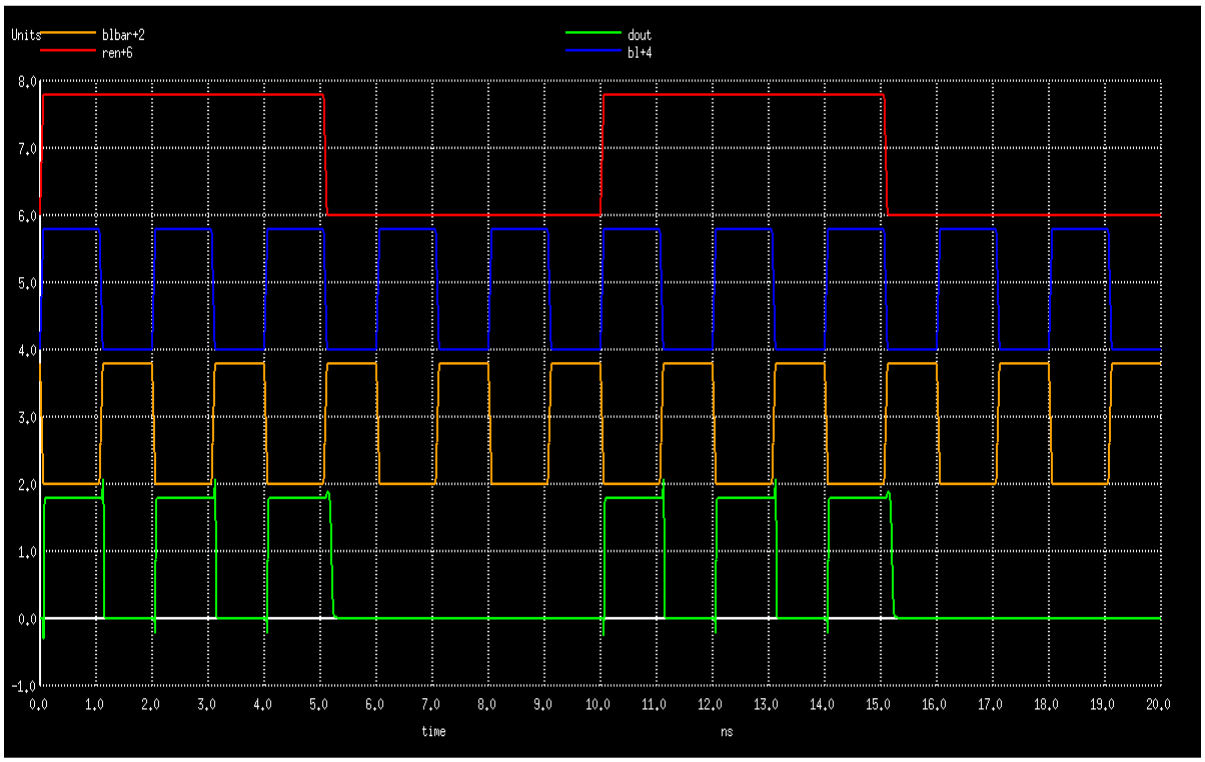


Figure 11: Sense amplifier simulation waveform.

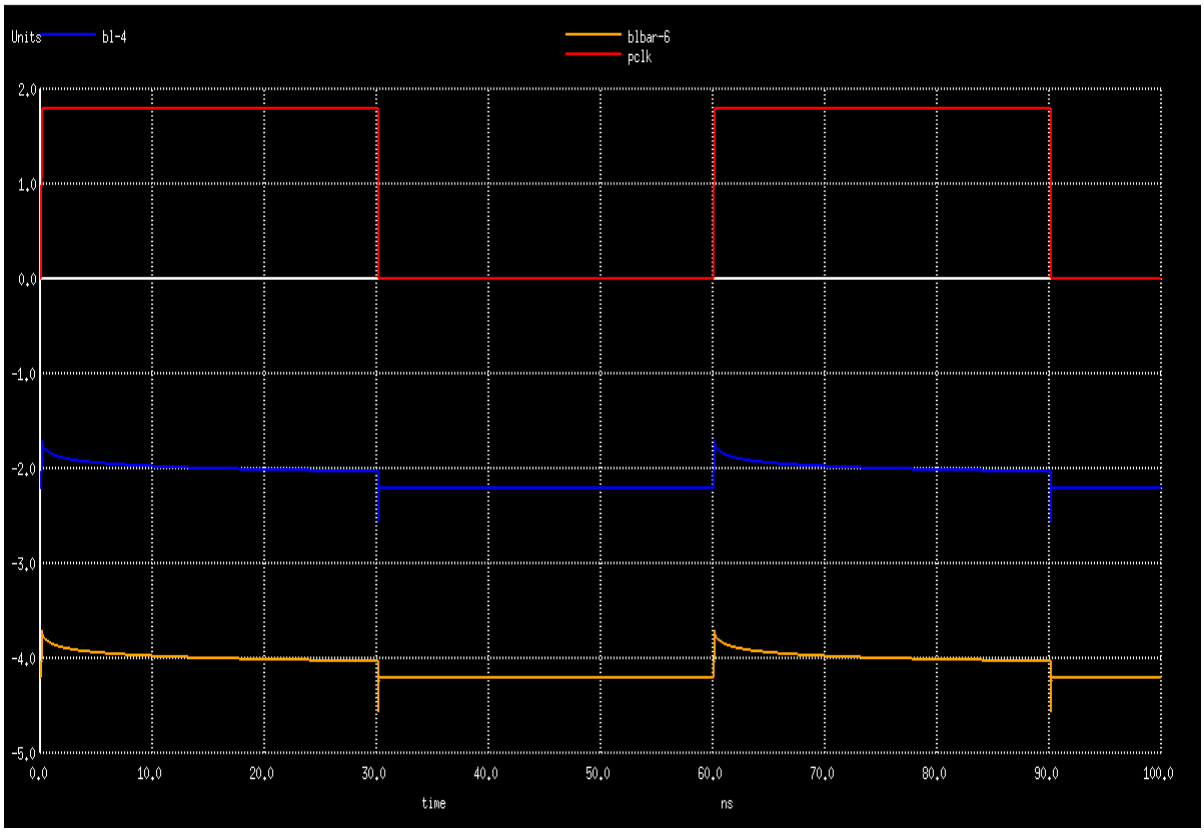


Figure 12: Precharge simulation waveform.

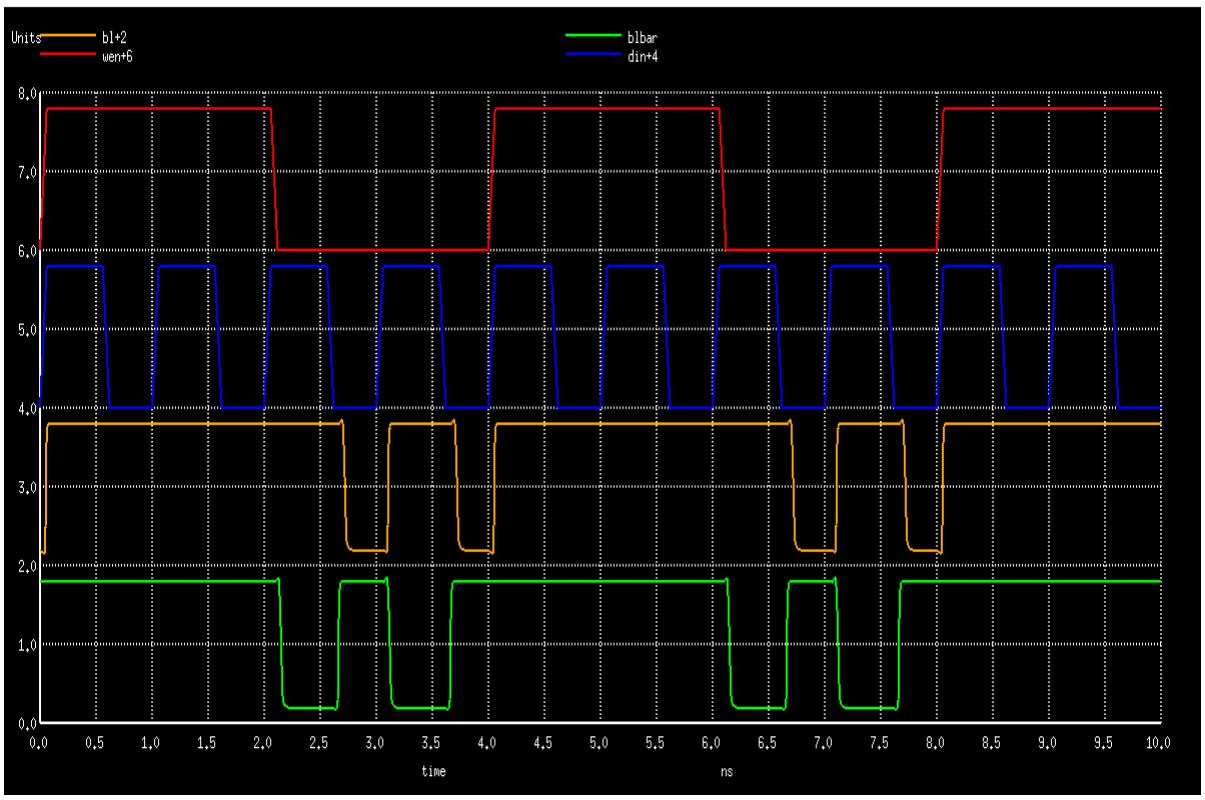


Figure 13: Write operation simulation.

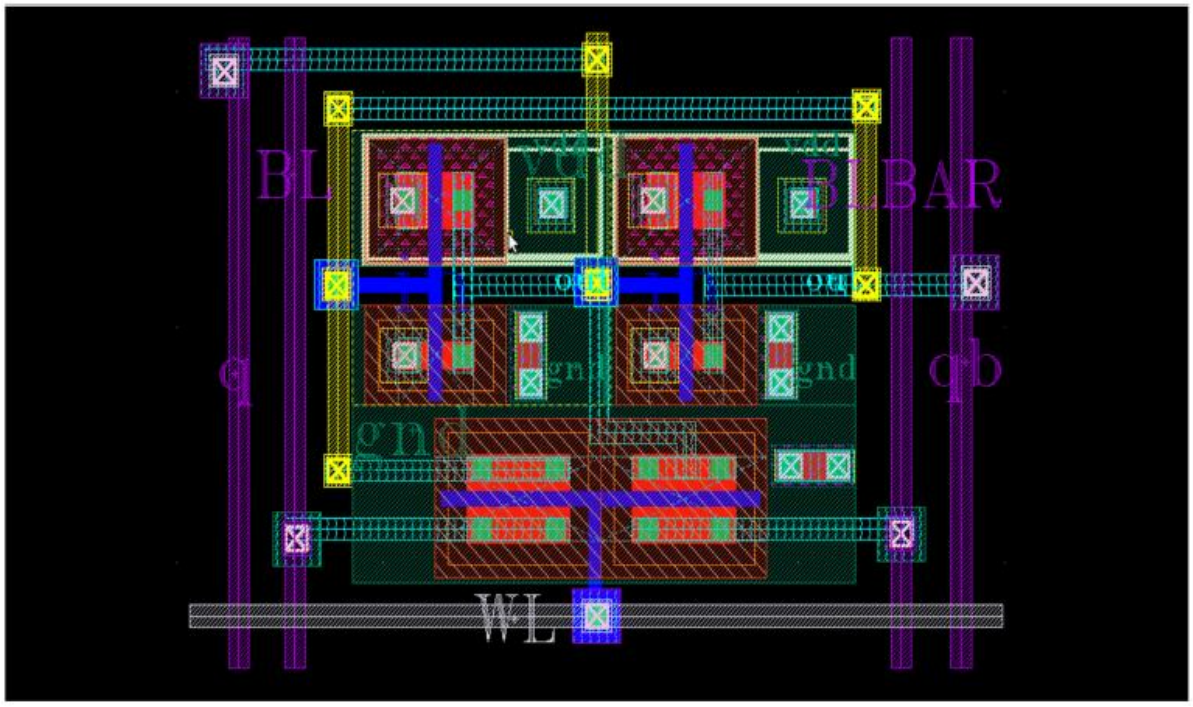


Figure 14: Layout of SRAM CELL.

Parameter	CMOS 6T SRAM cell
Technology (nm)	55
V_{DD} (V)	0.6
Area (um^2)	10.08
Normalized area in terms of 6T SRAM	1

Table1: Area Report SRAM Cell.

Parameter	CMOS 6T SRAM Cell
Technology (nm)	55
V_{DD} (V)	0.6
Leakage Current (pA)	185.57
Normalized Leakage current (in terms of 6T SRAM)	1

Table2:Leakge Current of SRAM cell.

V. Conclusion

SRAM memory with operating voltage of 1.8v and access time of less than 2.5ns is designed. The standard 1-bit 6T - SRAM cell consists of 6 transistors. It has pair of cross-coupled CMOS inverters and two NMOS access transistors(M5, M6). The NMOS transistors (M2, M4) and PMOS transistors(M1,M3) are driver and pull up transistors respectively. The area can be optimized by having a lesser number of cells and by replacing multiple cells with a single cell that includes both functionalities. From tables 1&2 our design can be used for a low leakage SRAM cell with improved stability and slight area overhead that can be tolerated in applications with tight constraints on stability and higher battery life.

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