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Single Phase Cascaded H-Bridge Inverter using Multi-Carrier PWM Technique for Grid power flow

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Abstract
Multilevel inverters typically have lower harmonic content in their output voltage and are utilised for high power and high voltage applications. Total harmonic distortion is greatly reduced by multilevel inverters with more levels. Using multicarrier PWM approaches, the output voltage's harmonic content is decreased. MATLAB/SIMULINK is used to create a five-level cascaded multilevel inverter with a multi-carrier PWM approach. The output voltage's total harmonic distortion is verified. Additionally, after adding grid integration requirements, the power flow from the inverter to the grid is certified and examined using LCL-Filter. By setting the reactive power to zero in MATLAB/SIMULINK, a Cascaded Multi-level inverter coupled to a single-phase grid is created to feed the grid.

Key words- Cascaded H-Bridge, Total Harmonic Distortion, Fast Fourier Transform, Pulse Width Modulation, Modulation Index, PQ Control.

1. Introduction

Industry has recently started to require more powerful machinery, which can now produce megawatts of power. A single power semiconductor switch cannot currently be connected directly to medium voltage grids. These factors have led to the development of a new family of multilayer inverters as a method of operating at greater voltage levels. The output voltages have more steps when the inverter's level count is increased, creating a staircase waveform with less harmonic distortion. The main PWM method used to drive multilevel inverters is sinusoidal, and a variety of multicarrier PWM methods can be used to reduce harmonic contents[1][4][8]. The basic output voltage is improved and total harmonic distortion is decreased using the multicarrier pulse width modulation cascaded multilevel inverter strategy[2][9].

Additionally, filters must be created in order to lower the system's undesired harmonics[3]. With improved functionality, multilevel inverters are highly helpful in both grid-connected and stand-alone applications[5]. Multilevel inverters have becoming increasingly prevalent in standalone applications, particularly in PV generation schemes. One of the most common inverter topologies used in standalone PV systems is the cascading H-bridge multilevel inverter[6]. Multilevel technology is appealing for PV applications due to the requirement of many sources on the dc side of the converter. Because the battery bank is integrated into the topology of the energy storage system, it can operate in either the inversion mode or the

battery charging mode. For better use of renewable energy sources, power generated by solar and wind energy is now connected to the grid. The grid or loads cannot directly use the electricity generated by renewable energy sources. An interface is employed between them using power electrical devices like DC-DC converters and DC-AC inverters, particularly MLIs. Pure sinusoidal waves or voltage/current with fewer harmonics can both be used to power the grid. The MLI design with LCL filter is used to achieve sinusoidal voltage and current with less harmonics, and the harmonic profile can also be enhanced[7]. Renewable energy sources, such as photovoltaic arrays with DC to DC converters, can provide the MLIs' DC input voltage sources[12].

2.Modelling of Inverters

2.1. Modelling Of Multilevel Inverter Using Pulse Generator

The power industry has shown a great deal of interest in multilayer inverters. In their new collection of features, which are ideal for use in reactive power compensation, they provide a novel approach. A more modern and sophisticated sort of power electronic converter called a multilevel inverter creates a specified output voltage from a number of levels of dc voltages as input. Multilevel inverters come in three different varieties. The first is the diode clamped multilevel inverter. 2. A multilevel inverter with flying capacitors. 3. Multilevel inverter with cascading. Cascaded multilevel inverters are utilised in this project because they require fewer components for each level and ((m-1)/2) H-bridges to build the model.

A single-phase full-bridge inverter is connected to each SDCS of identical magnitude. Different level inverters' ac terminal voltages are linked together in series. Each inverter level can produce one of three different voltage outputs—plus, minus, or zero—by combining the four switches, S1 through S4. The ac outputs of the various level full-bridge inverters are individually linked in series so that the resulting voltage waveform is the sum of the outputs of all the inverters. The formula m = 2s+1, where s is the total number of DC sources, determines the number of output phase voltage levels. There will be two SDCSs and two full-bridge cells in a five-level cascaded-inverter. The five level cascaded inverter's switching table is displayed below. In this instance, two full bridges are utilised and connected in a cascade. S1, S2, S3, and S4 are switches from the upper H-Bridge, whereas S5, S6, S7, and S8 are switches from the lower H-Bridge. We achieve 5 voltage levels by using the proper switching pattern: 2Vdc, Vdc, 0, - 2Vdc, and - Vdc. Here, Vdc equals 100V per. Interfacing with renewable energy sources is the multilevel inverter's most difficult use.

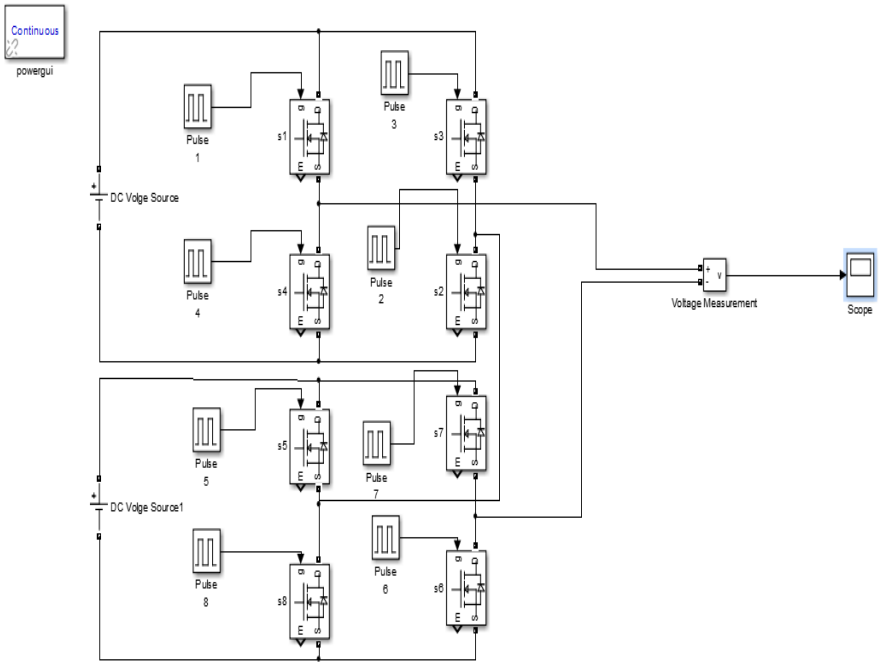

Figure 1. Five-Level Cascaded MLI Using Pulse Generator

Table 1- Switching table for five-level cascaded MLI

OUTPUT	S1	S2	S3	S4	S5	S6	S7	S8
$+V_{dc}$	1	1	0	0	1	0	1	0
$-V_{dc}$	0	0	1	1	0	1	0	1
0	0	0	0	0	0	0	0	0
$+2V_{dc}$	1	1	0	0	1	1	0	0
$-2V_{dc}$	0	0	1	1	0	0	1	1

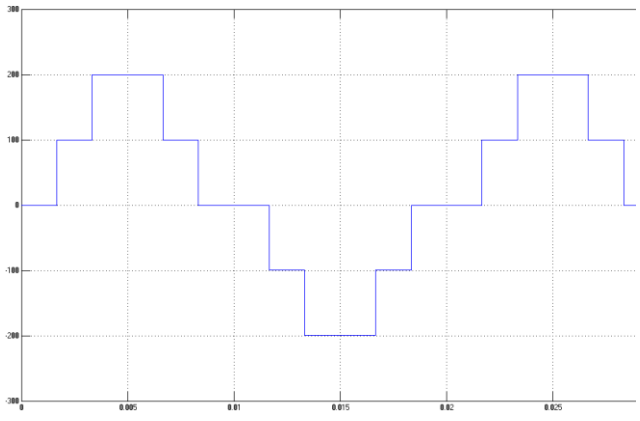

Figure 2. Five-Level Cascaded MLI output Using Pulse Generator

2.2 Modelling of Five Level Cascaded Inverter With Multicarrier Pwm Technique

To either transmit information across a communications channel or regulate the amount of power given to a load, pulse-width modulation (PWM) of a signal or power source entails the modification of its duty cycle. There are three methods: Phase disposition (PD): The phase of all carrier waveforms. All carrier waveforms above zero reference are in phase, and those below Reference are 180 degrees out of phase (phase opposition disposition, or POD). Every carrier waveform is 180 out of phase with its neighbouring carriers in an alternate phase disposition (APOD). In order to represent this, we used the PD PWM approach.

The DC voltages in the model below are each 100V. The carrier frequency is 5000Hz, while the reference frequency is 50Hz. The associated RL type load has values of R=20 and L=47mH, which results in 0.8 PF lagging. By adjusting the amplitude of the reference (modulating wave) signal, the modulation index (MI) in this case can be changed from 0.75 to 1.1.

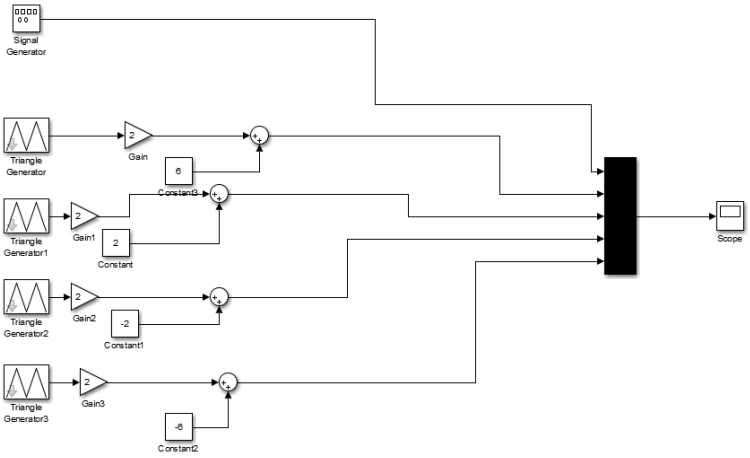

Figure 3. PD multicarrier gate pulse generation

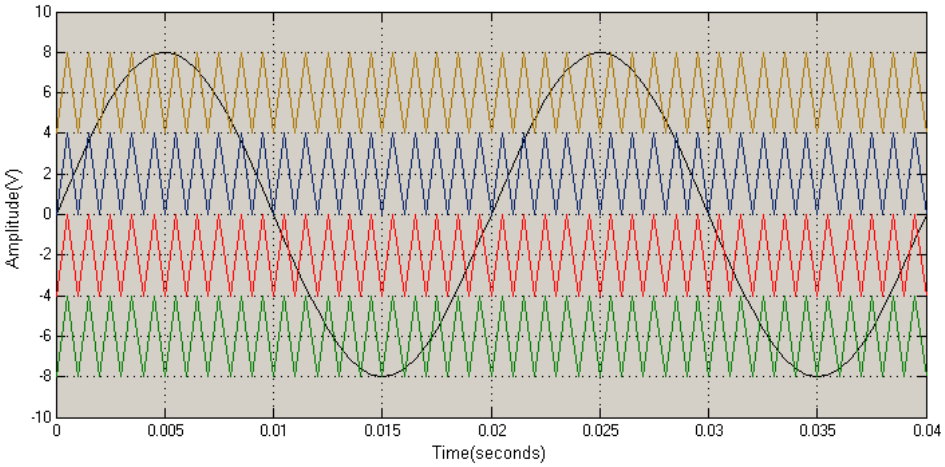

Figure.4. Representation of sine reference and triangular multi-carrier

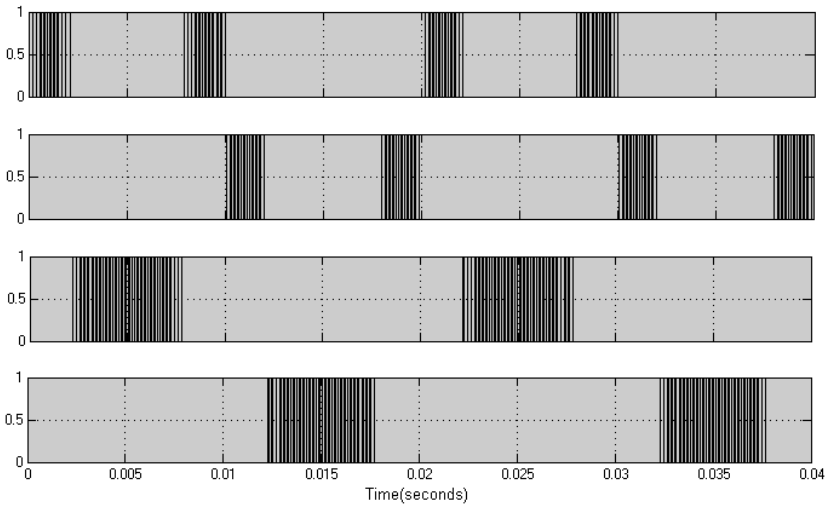

Figure.5. Pulse Generation for 8 switches (with complimentary pairs)

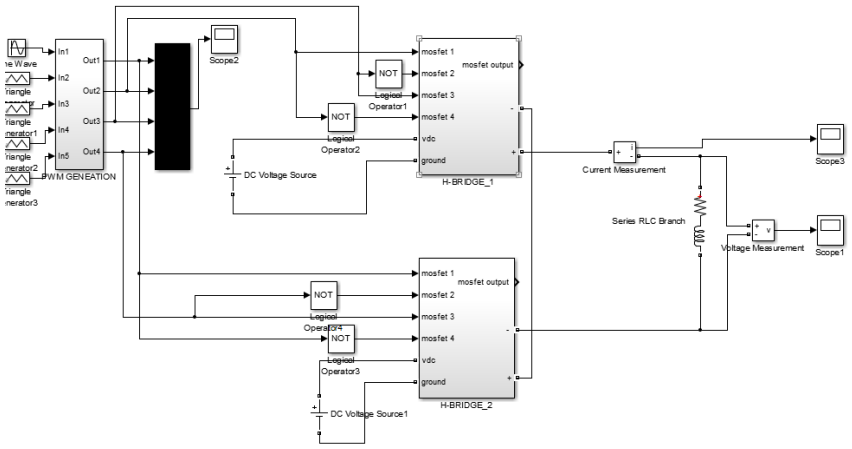

Figure 6. Simulink Model of the 5-level cascaded inverter with multicarrier PWM

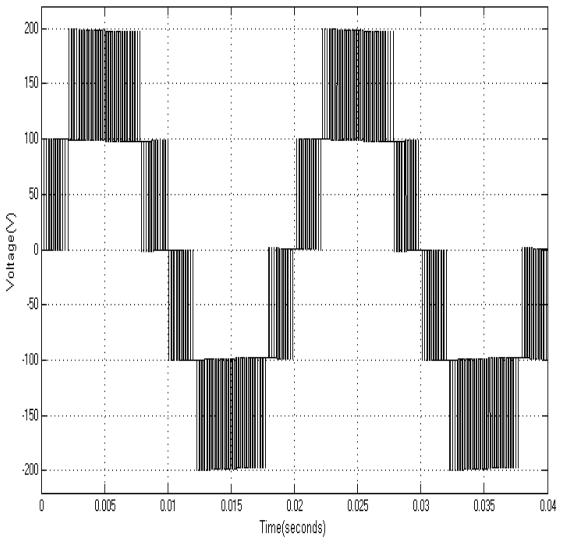

Figure.7. Output Voltage of the 5-level cascaded inverter With MC PWM

3.Discussion

3.1 Analysis of Total Harmonic Distortion Using FFT

The total harmonic distortion (THD) is a performance parameter which describes the quality of a waveform. It can be defined as the measure of closeness in shape between a waveform and its fundamental component. An inverter output consists of fundamental wave which is used to do real work and its harmonics (multiple of fundamental waveform) which causes heat loss in a system. Mathematically,the ratio of total harmonic content to the fundamental content in a waveform is called as THD.

$$\mathbf{THD} = \frac{\sum_{n=2,3..}^{\infty}(V_{on})^{1/2}}{V_{01}}$$

where

V_{on} - rms voltage of n th order waveform

n =2,3,4……

V_{01} - rms voltage of fundamental waveform

For an ideal inverter the THD is always 0%. To find the THD, a waveform is expressed in Fourier series as:

$$V_{out}=\frac{a_0}{2}+\sum_{n=1,2,3}^{\infty}(a_n \cos n\omega t+\sin n\omega t) \quad (2)$$

Where,

V_{out}- Fourier series expression of waveform

a_o , a_n, b_n are constants and are defined as,

$$a_0 = \frac{2}{T}\int_0^T V_o(t)dt \quad (3)$$

$$a_n = \frac{2}{T}\int_0^T V_o(t)\cos n\omega t\, dt \quad (4)$$

$$b_n = \frac{2}{T}\int_0^T V_o(t)\sin(n\omega t)\, dt \quad (5)$$

Where,

$V_0(t)$ is the output waveform as a periodic function of time.

T is the Time period of the output waveform.

By reducing the harmonics in the generated current, the output filter lowers the effects of semiconductor switching. Filters come in a variety of forms. Filter inductors attached to the inverter's output are the most basic variation. However, capacitor combinations like LC or LCL can also be employed. We utilised the L-C-L high pass filter in our design because it

attenuates inverter switching harmonics better than the L and L-C filters. For a 1 KW rated power,

Table 2 -LCL FILTER DESIGN VALUES

PARAMETERS	**VALUE**
L_i (inverter side)	8.137mH
L_g(grid side)	4.879mH
C_f Filter capacitance	3μF
R_d (damping Resistor)	10.623Ω

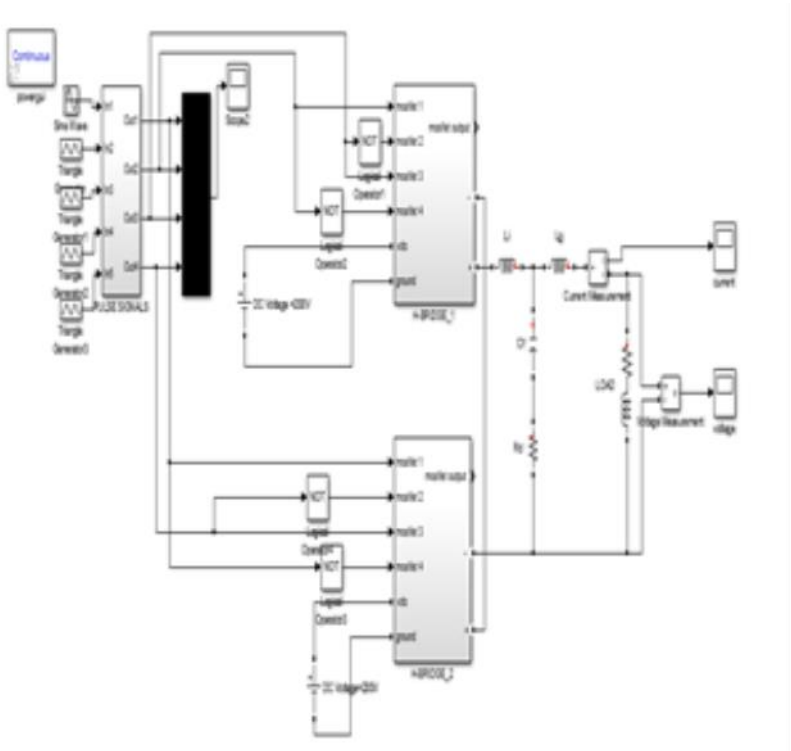

Figure 8. Simulink Model of the 5-level cascaded inverter with LCL-Filter

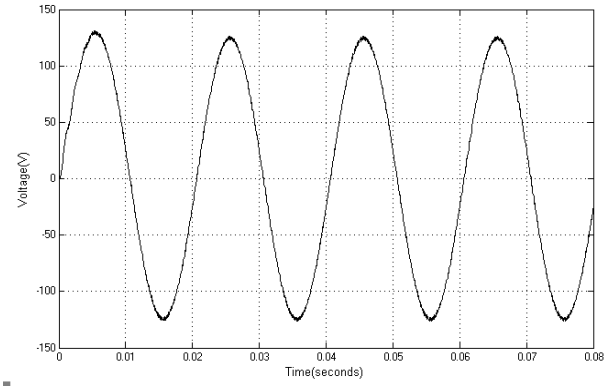

Figure 9. Output Voltage of the 5-level cascaded inverter With LCL-Filter

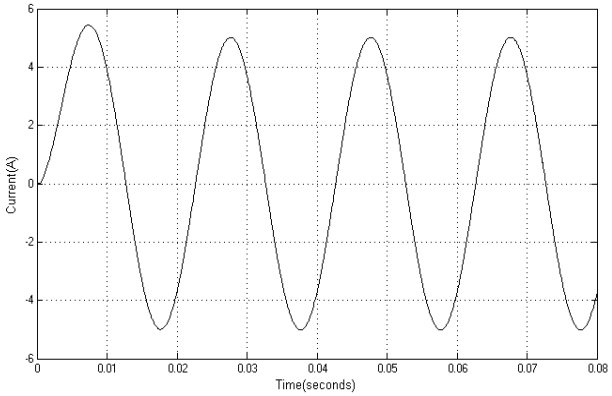

Figure 10. Output Current of the 5-level cascaded inverter With LCL-Filter

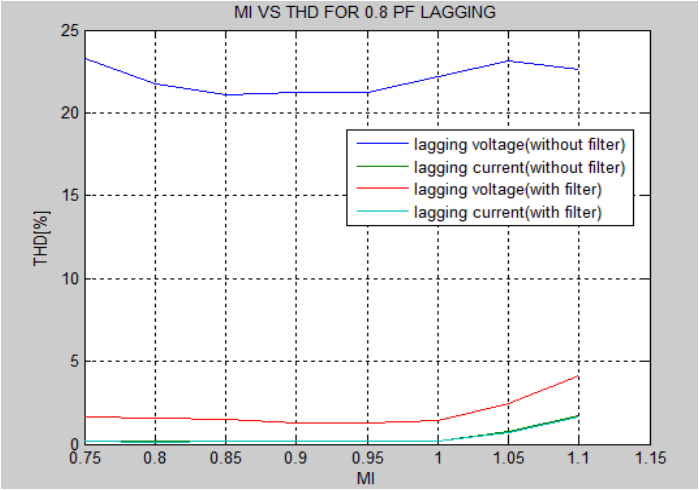

Figure 11. MI VS THD with LCL filter for 0.8 Lagging PF

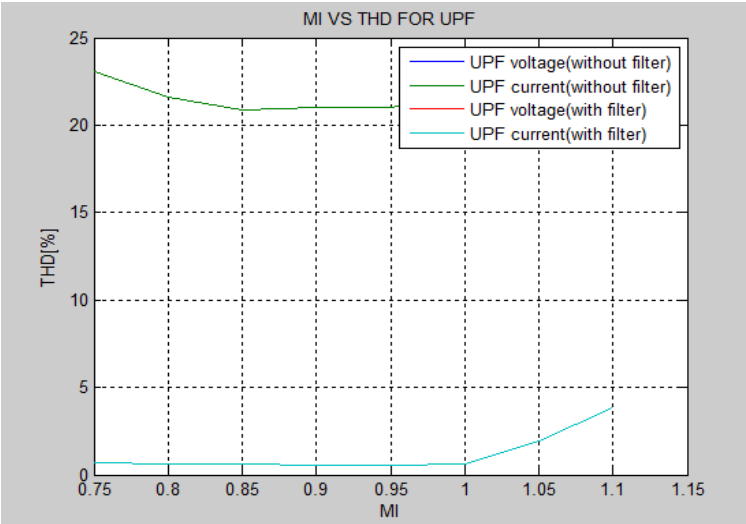

Figure 12.MI VS THD with LCL filter for UPF

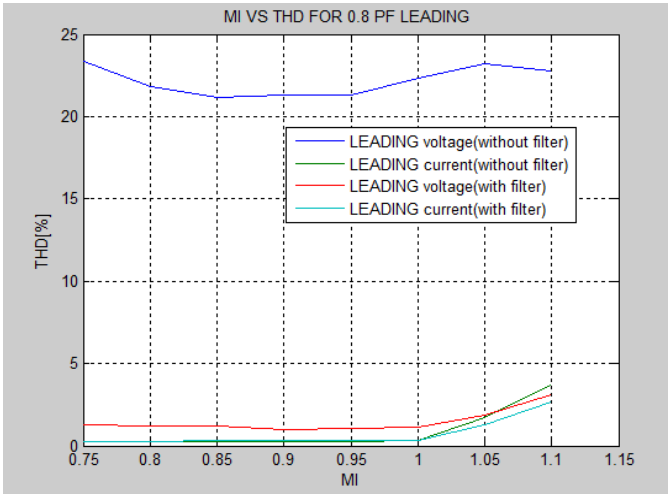

Figure 13. MI VS THD with LCL filter for 0.8 Leading PF

Table 3- THD COMPARISON FOR MI=0.8

LOAD	THD(%) Without filter	THD(%) With filter
R(UPF)	21.60	0.65
RL(LAGGING)	21.78	0.14
RLC(LEADING)	21.85	0.29

4.Results

4.1 Grid Connected Cascaded MLI With LCL-Filter

When integrating the grid, various restrictions are taken into consideration. The Lg inductor in the LCL filter circuit acts as a decoupling inductor, which is required to regulate the power flow from the inverter to the grid. To allow the grid to receive inverter current, V_{inv} must lead the Vgrid at a specific angle. I_{inv}(Iout) needs to stay in sync with the V_{grid}. This is

accomplished by changing the modulating wave's phase angle (reference sine wave). To operate at unity power factor, this is done. (The reactive power is Zero).

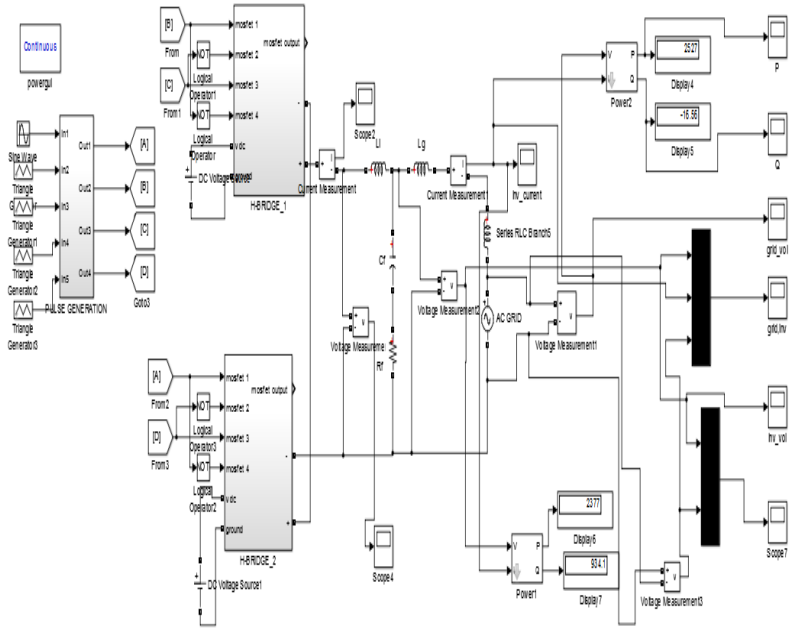

Figure 14. Simulation Model of grid connected cascaded MLI

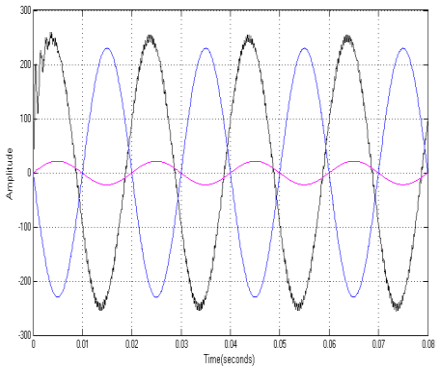

Figure 15. Waveforms of Vinv, Iinv ,Vgrid

From above, it is observed that V_{inv} leads V_{grid} and $V_{grid,}$ I_{inv} are in phase with each other which is the requirement for the power flow.

By using the PI controller tuning, PQ control is done. The K_p ,K_i values are as follows: 0.001, 0.3 respectively. The real power and reactive power are set to 1000 Watts and 0 Watts respectively.

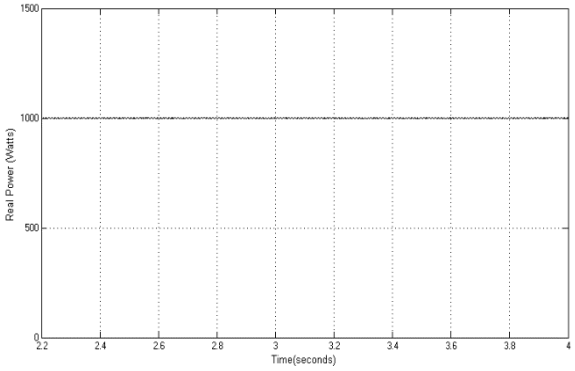

Figure 16. Real power is set to 1000 Watts

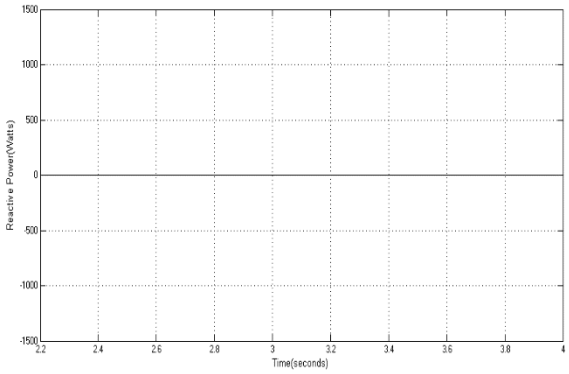

Figure 17. Reactive power is set to 0 Watts

5.Conclusion

The cascaded MLI is modeled with Phase disposition (PD) Multi-carrier pulse width modulation technique. The harmonic analysis is done and LCL filter is used to reduce the THD. Finally, Grid is connected to the cascaded MLI with suitable constraints to enable the inverter output current to flow through the grid. Through phase angle adjustment Unity power factor is achieved in the grid such that reactive power Q=0 is maintained. The PQ control is done using the PI controller tuning in the closed loop domain. The present work can be extended to include PV array as a DC source.

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